PLLatinum Sim User Guide

Last Updated 5/16/2025

Document Revision History

Date	Author	Descriptions
1/30/2022	Dean Banerjee	Initial Document Created
4/4/2022	Dean Banerjee	Updated Active Filter Information Updated N Divider Fractional Settings Updated Spur Section
8/29/2022	Dean Banerjee	Added cascaded simulation descriptions.
4/21/2023	Dean Banerjee	Updated discrete lock time modeling descriptions. Added updates for Fastlock, update pictures for phase noise & filter
4/1/2024	Dean Banerjee	Added cascade noise analysis
5/16/2025	Dean Banerjee	Updated phase noise for UsePoints option

Table of Contents

1 High Level Overview

1.1 Scope of PLLatinum Sim

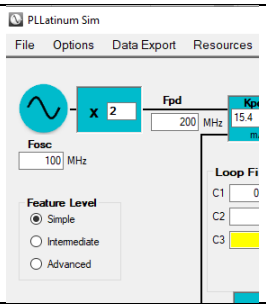
- ***Select Devices*** by specifying criteria such as output frequency, required features, device type, current, chip area, and noise performance. These criteria are focused on the PLL in the device. At the time of these instructions being written, buffers & divider buffers are just starting to be added. The device selection is focused on the PLL portion of integrated devices. For instance, for a device with integrated PLL + Mixer (LMX8410L), the tool only focuses on the PLL portion of this device
- ***Set Up Devices*** on the main setup tab. This includes frequencies, charge pump current, option to manually enter loop filter components, and more. There is some feedback given regarding frequencies and divider ranges if they are not legal for a device, but the diagram is a high-level abstracted view of the device and does not include the full complexity of devices. In order to see the full detail of a device, use the Texas Instruments TICSPro tool that has more detailed device level diagrams and also generates registers
- ***Design Loop Filter*** based on loop bandwidth and optionally parameters such as phase margin, gamma, and pole ratios. An advanced optimizer also can design based on optimizing one parameter subject to constraints, such as designing for the lowest possible jitter subject to the constraint that the phase noise at 1 MHz offset is -120 dBc/Hz or better
- ***Simulate Loop Filter*** for phase noise, spurs (including fractional spurs), lock time (including VCO calibration options for discrete time modeling), and bode plot. The simulations are very powerful and based on mathematical models that use performance indices that are extracted from actual measurement during characterization of the device.

1.2 Typical Simulation Accuracy

The actual performance can vary from the simulation and can also vary over process, voltage, and temperature. There will be some mismatch between simulation and actual and this can vary significantly based on setup conditions. ***This table is only a rough estimate and simulation accuracy results will vary with setup and with the device being simulated.***

Tab	Parameter	Typical Simulation Accuracy	Common Factors Leading to Simulation Accuracy Greater than Stated Value
Filter Design	Loop Bandwidth	<10%	• VCO gain, charge pump gain, or loop filter components stated in simulation not matching the actual values • For active filters, non-ideal op-amp properties
Phase Noise	Spot phase noise	<2 dB	• Input reference noise not entered correctly or not at all • Slow slew rate on input reference • VCO high order capacitor too small (tool gives warning)
Spurs	All spurs	<15 dB	• Slow slew rate on input reference • Crosstalk on board/power supply • Multiple factors not modeled impacting spur at same offset • Comment: Simulation/Actual mismatch can vary wildly based on spur type and setup. For a given spur and setup, variation is typically <5 dB, but spurs are very sensitive to setup, and PLLatinum Sim does not model all of this
Lock Time	VCO Calibration Time	<15%	• VCO programmable settings • Board/supply pin crosstalk • The models themselves.
	Analog Lock time	<15%	• Mismatch for Kvco, Kpd, or components • Railing at power supply • Discrete phase detector sampling action • Dielectric absorption in capacitors

1.3 Feature Level

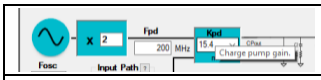


The Feature Level allows the user to select the details shown. Selection the Advanced option will show the maximum details, although this may be overwhelming to the user. For this reason, there are also the Intermediate and Simple feature levels that hide details and make assumptions about the parameters that are hidden. In the Simple feature level, far less details are shown and assumptions are made about parameters that are not show.

What	Basic Feature Level	Intermediate Feature Level	Advanced Feature Level
Menu Bar	Load/Save Design, Import from TICSPro, Options for Main Diagram and Filter Designer Tab, Export Design to Excel and traces as text files, Links to help and product folders and E2E.		
Part Selection Tab	Selects the device based on frequency, device type, and features	Allows use to also screen based on current, PLL figure of merit, VCO figure of merit, and Package size	
Main Diagram	Set up the frequencies and settings for the selected device	VCO Core selection	Fractional Settings and input path Input Path
Filter Designer Tab	Design loop filter based on loop bandwidth. Allows passive and active filters and theoretical ideal filters	Also choose loop bandwidth	Choose pole ratios and gamma optimization factor. Advanced filter optimizer.
Phase Noise Tab	Model phase noise and jitter. Set up graph and integration limits. Graph phase noise based on causes.	Phase noise import, other integrated noise metrics, spot phase noise	Distribution path noise, VCO noise metric override
Spurs tab	Graph setup	Integrated spur metrics	MASH_Seed, Spur mechanisms, spur decomposition chart
Lock Time Tab	Graph Setup Analog Lock time VCO Calibration	VCO Calibration Start	Lock Time to Phase Discrete Lock Time modeling
Bode Plot Tab	Graph Setup	Parameters Spot Metrics	Closed Loop Parameters

Pictures in this document are shown using the Advanced Feature Level in order to show all of the capability. Realize that in Basic or Intermediate Feature Level, some features will not be visible.

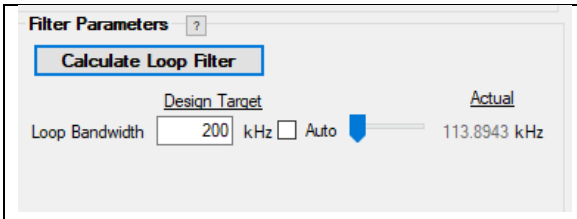
1.4 Tool Tips and Warning Boxes

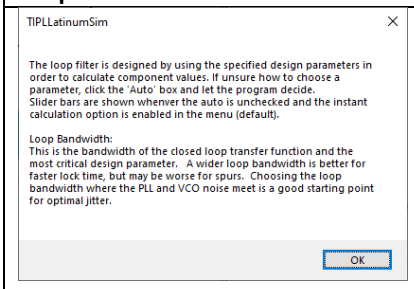
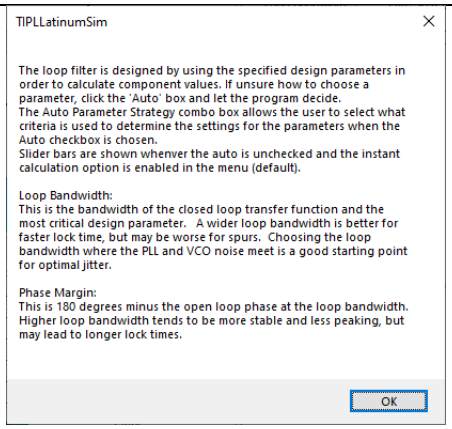
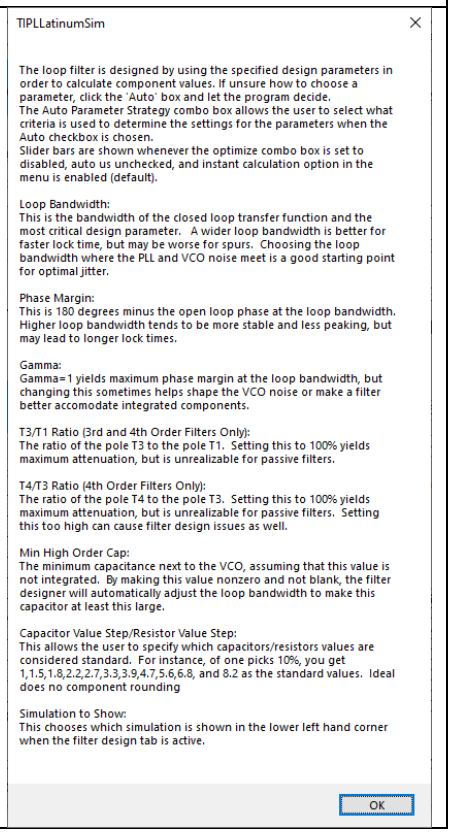
	Several controls and entry boxes will show tool tips when the mouse pointer hovers over them.
	Boxes that change yellow means there is a warning, red means a more severe warning. Mouse over the box to see the warning. If no warning message appears, try selecting the box and pressing <enter>.

1.5 Other Resources that Interact well with PLLatinum Sim

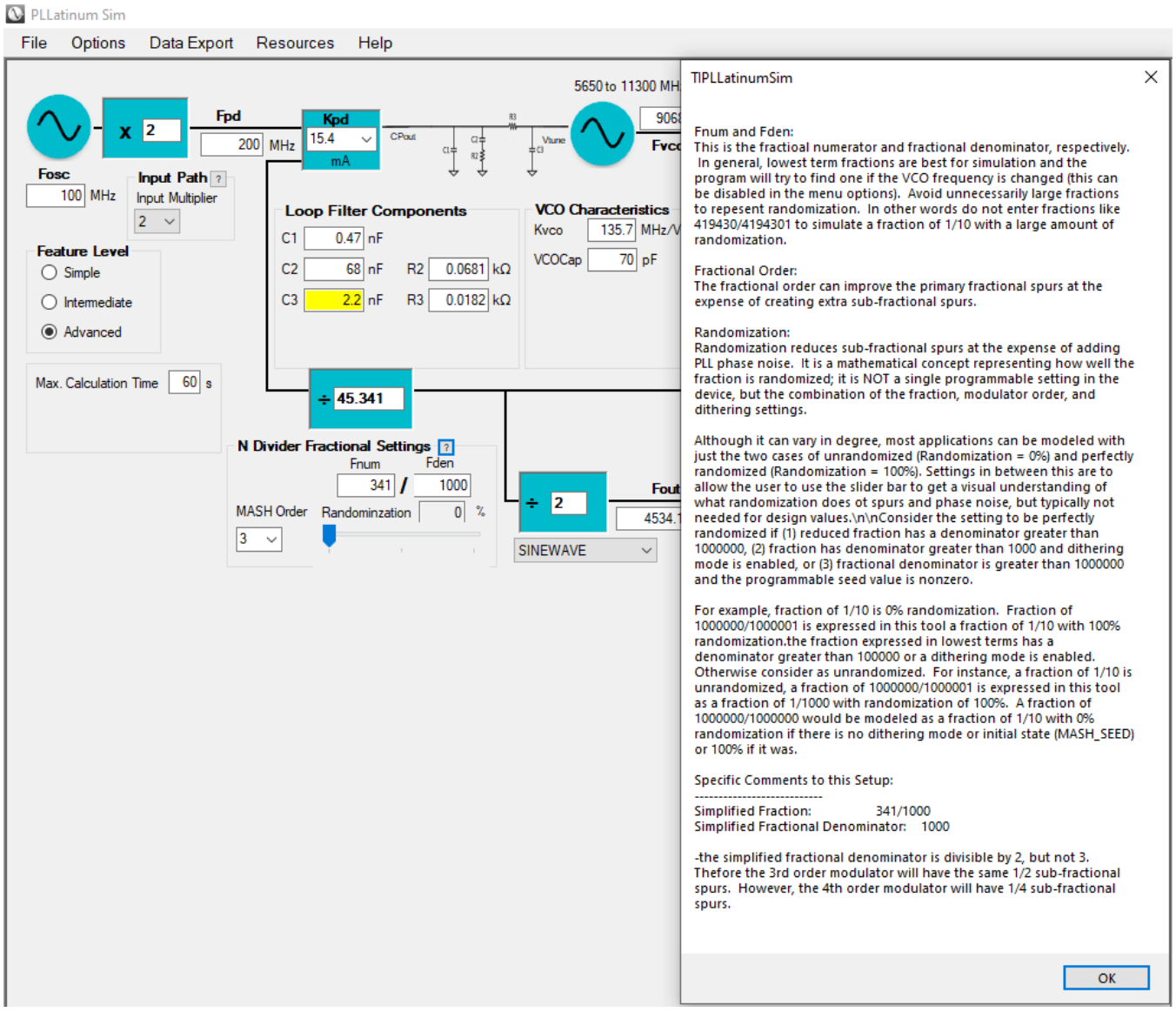
- *PLL Performance, Simulation, and Design* by Dean Banerjee includes formulas and concepts that PLLatinum Sim is based off of
- The Texas Instruments TICSPro tool is excellent for configuring registers and PLLatinum Sim supports importing TICSPro files for many Texas Instruments devices

1.6 Help Boxes with Built in Help

	The PLLatinum Sim tool is being upgraded often and it includes useful, context sensitive built in help based on the user level settings of the device. The tool may be updated after these instructions are created, but the online help will get upgraded with the tool. There are a great many concepts that are not obvious. ***Do NOT forget to click on the "?" for help***!

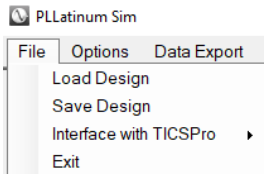
Simple Feature Level	Intermediate Feature Level	Advanced Feature Level
		

Many of these help boxes have very comprehensive and context sensitive help. There are many concepts that are complicated that are explained in these text boxes. The help box for the N divider is a good example.



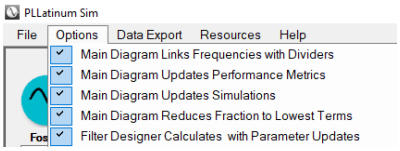
2 Menu Options

2.1 File

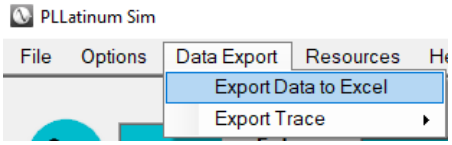
	***Load Design/Save Design*** allows a file to be loaded or saved in a *.sim format (a format specific to PLLatinum Sim). If an older version of a saved file is detected, then PLLatinum Sim will convert it and alert the user ***Interface with TICSPro*** allows a TICSPro file (*.tcs format) to be imported so that the frequencies, formats, charge pump current, and other features mainly on the main setup screen can be updated. There is also an option to "Add Filter to TICSPRo". This option just adds the loop filter information to the *.tcs file from TICSPro. So that a single file can have the loop filter information and programmable settings. However, this does nothing special when it is loaded in TICSPro.

2.2 Options

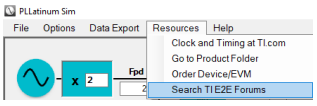
These options are straightforward and many of them have been already discussed. Then can be enabled or disabled.

	***Main Diagram …*** The top four options apply to the main diagram. The defaults are that it updates frequencies, performance, simulations, and fractions to lowest terms. But sometimes this is undesirable, so this feature can be disabled. ***Filter Designer Calculates with Parameter Updates*** will automatically calculate the loop filter when a parameter is changed without requiring the user to press the "Calculate Loop Filter" button

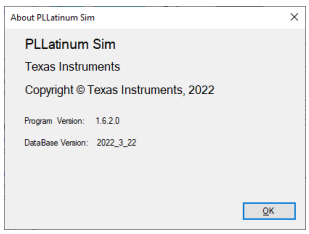
2.3 Data Export

	***Export to Excel*** exports the whole design into one elegant workbook with separate tabs for each tab. As a bonus, it gives some additional information not in the GUI, such as the MASH sequence for fractional divides ***Export Trace*** exports phase noise and lock time traces as text files

2.4 Resources

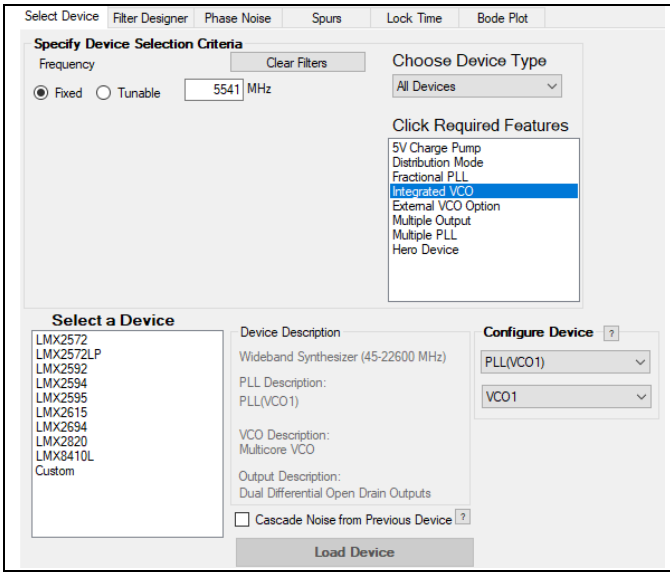
	The resources menu option has links to product folders and websites. The ***Search TI E2E*** forums option automatically goes to the Texas Instruments E2E (Engineer to Engineer) website and searches for posts on the currently selected device.

2.5 Help

		Help-> Users Guide opens the users guide from the program. Help->About option displays the program version information. The program version gives an indication of when the source code of the program was updated. There is also a database version that indicates when the database was updated as it is possible for the PLLatinum Sim database to be updated without updating the source code.

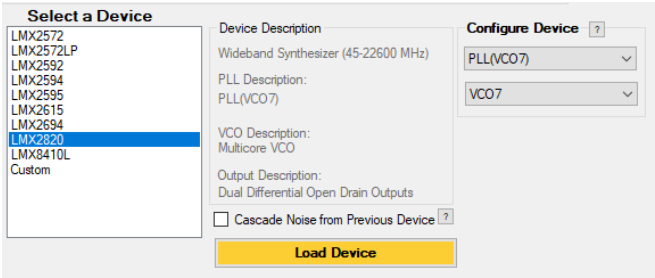
3 Select Device Tab

3.1 Optionally enter the frequency, device type, features, and use scroll bars



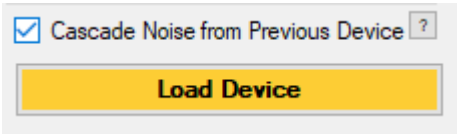
To search devices, a fixed or tunable frequency may be entered, but is not required. It is also possible to use the slider bars to screen for current, PLL figure of merit, VCO figure of merit, or package size. Using these tools, one can quickly narrow down the device choices for the application.

3.2 Click on the device, configure the device, cascade noise if desired and press “Load Device” button



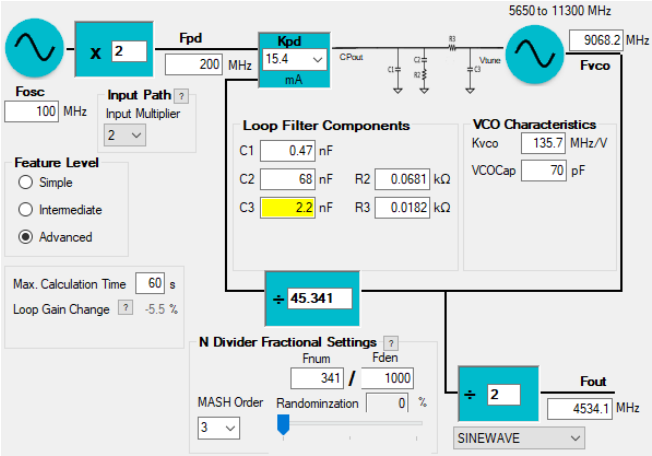
When a device is clicked on, the configure device box may appear and it may show different options. A default option is selected, but can be changed. This default is based on choosing a PLL and VCO core that hits the desired frequencies. For multi-core VCO devices, one can select the core. For devices with more than one PLL, you can choose which PLL. Be sure this is the correct PLL before you press the “Load Device” button.

For dual PLLs or dual loop jitter cleaners, be sure the desired PLL is selected. You can only simulate one PLL at a time.



If the “Cascascade Noise from Previous Device” option is checked a the time that the <Load Device> button is pressed, then phase noise and frequency for the output at the time before the <Load Device> button was pressed becomes the frequency and imported phase noise for the new Fosc frequency after the <Load Device> button is pressed.

4 Main Diagram



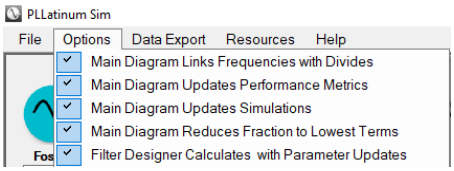
Frequencies, loop filter component values, charge pump gain, divide/multiply values, VCO characteristics, and N divider settings can be entered in the white boxes. Output format, input multiplier, and charge pump gain (also can be directly entered) can be selected from a list of options. Divide and multiply signs can be toggled by clicking on them.

When the loop filter is designed, these components are updated. It is also possible to enter the existing components and conditions for an existing design in order to simulate its performance.

Note that this setup is with the LMX2820 and is used in many of the examples in this document.

4.1 Menu Options for Main Diagram

However, if the GUI is fighting your entries, you can disable the options in the main menu. The top 4 options on the menu apply to the main diagram; the last one applies to the filter designer tab.



Main Diagram Links Frequencies with Divides causes any update of a frequency on the main screen to update the divides (or multiplies) and the other way around as well. In some cases, such as when the VCO frequency is mixed down before going to the N divider, this option needs to be disabled.

Main Diagram Updates Performance Metrics causes updates on the main screen such as frequencies, divides, charge pump gain, VCO core, MASH Order, and output format to update performance metrics.

Main Diagram Updates Simulations causes any update of a frequency on the main to trigger simulations to be calculated. If the simulation takes a long time, then it might make sense to disable this option

Main Diagram Reduces Fractions to Lowest Terms reduces fractions to lowest terms. In cases where there is simulation value in not reducing the fraction, such as a nonzero MASH_SEED, it may make sense to disable this option.

4.2 Feature Level, Max Calculation Time, and Loop Gain Change

- ***Feature Level*** allows user to show more or less details. Default values are set for unseen parameters
- ***Max. Calculation Time*** limits the amount of time that is allowed for the advanced filter optimizer, fractional spur calculations, and discrete lock time modeling.
- ***Loop Gain Change***: This gives an indication of how much the loop gain (Kpd*Kvco/N) has changed from the value when the filter was designed. A large change suggests that the filter may be unoptimized and one should re-design the loop filter or adjust the charge pump gain to compensate for the change in loop gain.

4.3 N Divider Fractional Settings

The N divider shown is a calculated value and can be the combination of several components including the PreN divider and fractional circuitry.

- ***PreN Divider*** is a fixed divider that some devices have that contributes to the total N divide value. These are sometimes necessary to reduce the frequency or for phase synchronization. A PreN divider can impact the impact of the fraction and fractional spurs
- ***MASH Order*** is the order of the fractional modulator. This impacts spur levels and offsets. One can change this and dynamically see the impact it has on phase noise and spurs.
- ***Randomization*** is an abstract concept necessary that represents how well the fraction is randomized and is necessary for the modeling of fractional noise and spurs. There is no programmable setting in devices called "Randomization" and there is no simple closed form equation to calculate "% randomization". Randomization relates to how long the fractional sequence is before it repeats and this can be increased in devices by using dithering, nonzero MASH_SEED, or representing the fraction in larger irreducible terms. In general, reduced fractional denominator larger than one million or even one billion would be needed to be considered 100% randomized. In most cases, it makes sense to represent randomization as either 0% or 100%, but there might be some cases where an intermediate value might make sense. Also, the ability to move the slider bar to intermediate states gives the user a more visual understanding of the impact of dithering. The following table gives an idea of how randomization might be chosen.
- ***Fnum and Fden*** represent the fractional numerator and denominator. They are reduced to lowest terms if so instructed by the menu option. This is done by dividing out the greatest common divisor of Fnum and Fden.

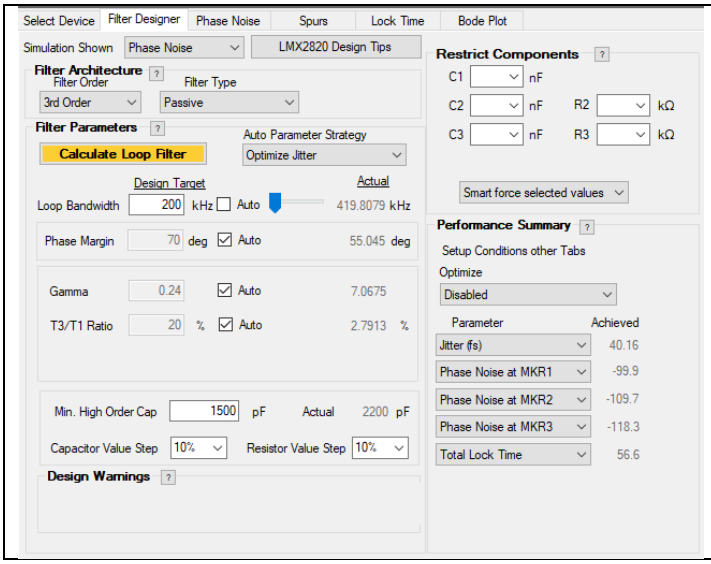
  For the purposes of fractional spur calculations only, the fraction is reduced internally to lowest terms, however, the greatest common divisor must also divide MASH_SEED. The fraction may also be internally reduced when calculating spurs. For the spur calculations, the fraction is reduced to lowest terms, but after this, there is a limit to the denominator size based on the MASH_ORDER and factors in the reduced fractional denominator.

		Maximum Fraction Denominator for Spur Calculations			
		MASH_ORDER=1	**MASH_ORDER=2**	**MASH_ORDER=3**	**MASH_ORDER=4**
Reduced Fractional Denominator	Not divisible by 2 or 3	64000	64000	64000	64000
	Divisible by 2, but not 3	64000	32000	32000	16000
	Divisible by 3, but not 2	64000	64000	21333	21333
	Divisible by both 2 and 3	64000	32000	10666	5333

Below is a table with some examples one might model actual fractional settings in PLLatinum Sim.

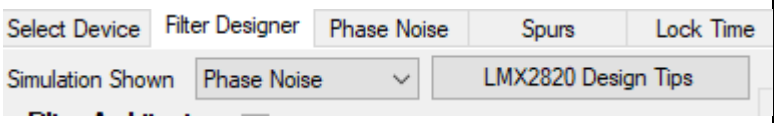
Actual Device Settings	**PLLatinum Sim Representation**
Fraction = 1/1000	Fnum=1 Fden=1000 Randomomization=0%
Fraction = 1000000/1000000000 MASH_SEED=0	
Fraction = 1000000/1000000000 MASH_SEED=1	Fnum=1 Fden = 1000 Randomomization=100%
Fraction = 1000000/1000000000 Dithering Mode = Strong Dithering	
Fraction = 1000000/1000000001 MASH_SEED=0	
Fraction = 1001/1000000 MASH_ORDER=3	Fnum = 1 Fden = 1000 Randomization = 50%

5 Filter Designer Tab

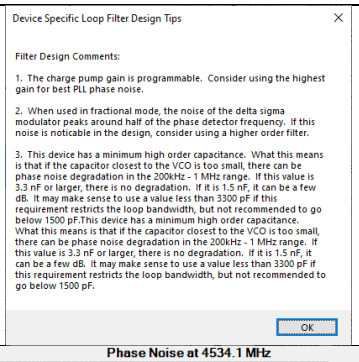


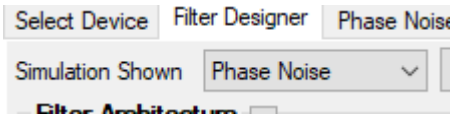
The Filter Designer tab gives maximum power for filter optimization. Note that in Advanced Mode, the “Performance Summary” group box changes to the optimizer settings when the “Optimize” combo box is set to anything other than “Disabled”.

5.1 Design Tips and Simulation Shown

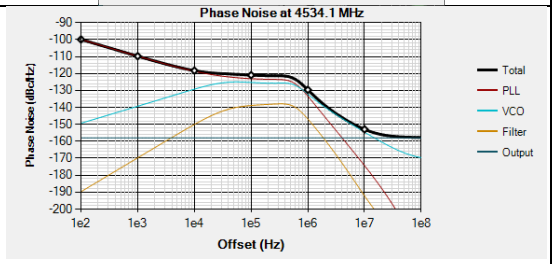


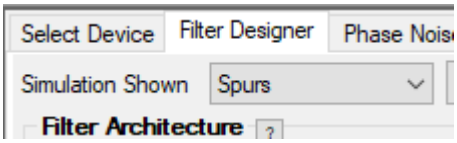
The ***Design Tips*** box gives part specific loop filter design information when clicked.

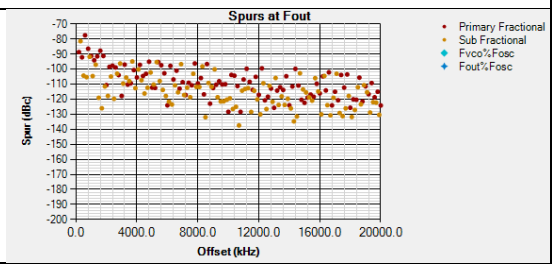




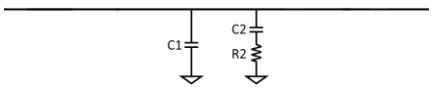
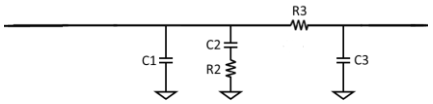
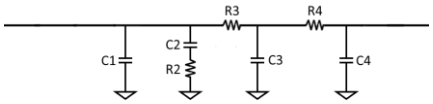
The simulation chart shown on the filter designer tab can be changed. This us useful for the user to directly see the impact of design parameters.



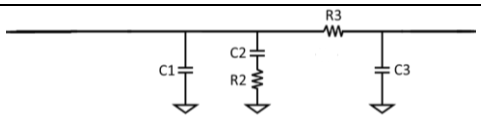
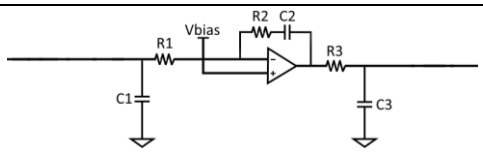
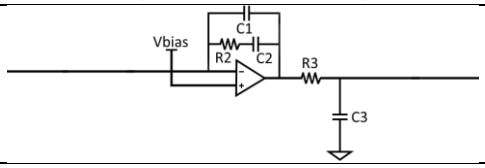
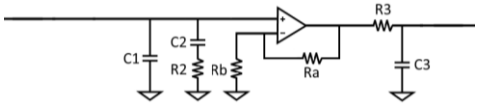
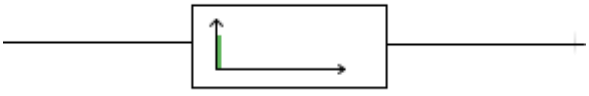
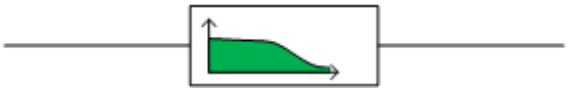




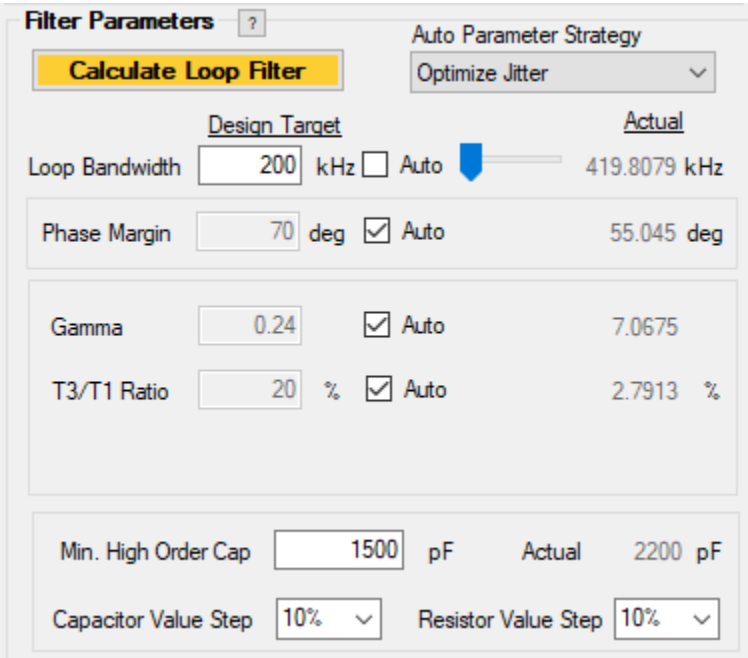
5.3 Filter Order and Filter Type

Filter Architecture Filter Order: 2nd Order Filter Type: Passive	
Filter Architecture Filter Order: 3rd Order Filter Type: Passive	
Filter Architecture Filter Order: 4th Order Filter Type: Passive	

5.4 Filter Type

Passive Filter has only capacitors and resistors	
Active Type A Filter with op amp to boost voltage. C1 & R1 reduce speed requirements on op amp while still allowing charge pump to operate at mid voltage	
Active Type B Filter with op amp to boost voltage. Less optimal that Active A or Active C, but might be easier for board layout that can accommodate both active and passive filter	
Active Type C Filter with op amp to boost voltage. Most intuitive approach where a simple voltage gain is used and also least demanding for the op amp. However, this approach also multiplies the voltage noise of the op amp.	
Infinite Loop Bandwidth Theoretical filter that passes all in-band noise sources and eliminates all out-band noise sources. Useful analyze input reference and PLL noise.	
0 Hz Bandwidth Theoretical filter that passes all out-band noise sources and eliminates all in-band sources. Useful to analyze VCO phase noise.	
Brick Wall Theoretical filter passes in-band sources in the loop bandwidth and eliminates them outside the loop bandwidth. Vise versa for out-band sources. Good to set a limit for best possible jitter.	
Ideal NonComponent Ideal filter that ignores component restrictions and the restrictions they put on parameters.	

5.5 Filter Parameters

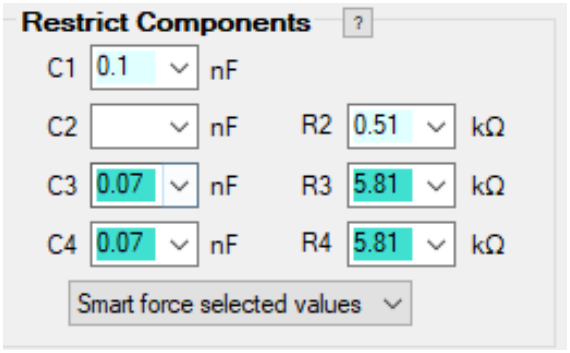
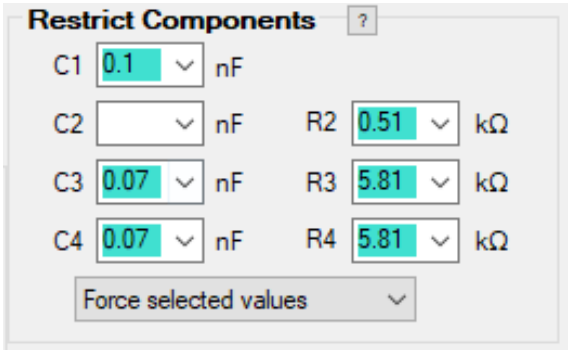
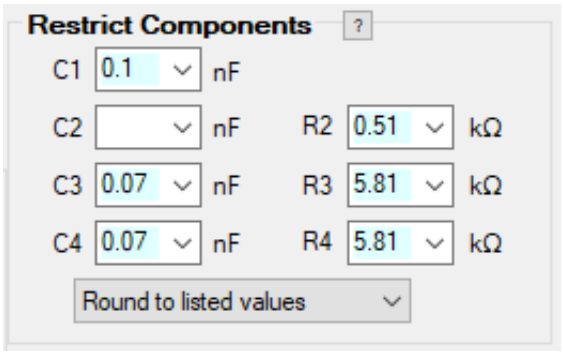
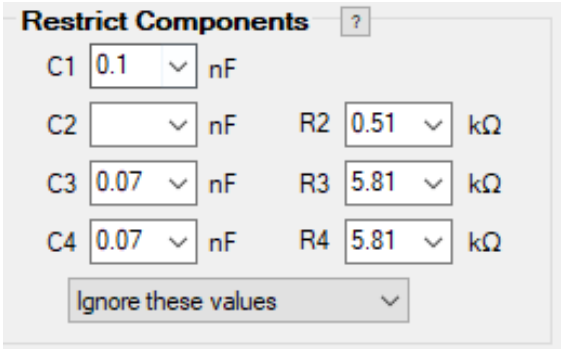


The Filter Parameters group box has the filter design parameters of loop bandwidth, phase margin, gamma, and pole ratios.

- Auto Parameter Strategy and Auto Check boxes
  - The Auto Parameter Strategy chooses the method for choosing Loop Bandwidth, Phase Margin, Gamma, T3/T1 ratio, or T4/T3 ratio when the "Auto" checkbox is chosen and not in advanced optimizer mode. Options are Optimize Jitter, Maximize Loop Bandwidth, Minimize Loop Bandwidth, or Balance for Spurs.
  - Note that in Advanced Optimizer is used, the Auto Parameter Strategy combo box disappears
- Sliders
  - When not using the advanced optimizer and the Auto checkbox is selected, this allows the user to slide the parameter value to see interactively with the graphs what the impact is.
- Actual Value
  - The design target specifies the design target, but the actual value may be different due to component rounding.
- Min High Order Cap
  - The high order capacitor is the one closest to the VCO. It is desirable for this not to be too small so that it is not swamped out by the VCO input capacitance. Also, some devices with integrated VCO get phase noise degradation if this value is too small. PLLatinum Sim will reduce the loop bandwidth to achieve this value if necessary. The loop bandwidth can be restricted due to the Min High Order Cap or VCO input capacitance.
- Capacitor Value Step/Resistor Value Step
  - The design target specifies the design target, but the actual value may be different due to component rounding.
- Design Warnings
  - When there is some non-ideal issue that happens when the filter is designed, a design warning will appear. Be sure to click on the "?" box to see the meaning of this warning

5.6 Restrict Components

Some devices have partially integrated loop filters where one is restricted to a discrete set of values. Other times, a use might want to force a particular component value. ***These forced components are for the loop filter design, not the actual values that are being simulated (these are on the main diagram).*** Dark teal indicates the value is forced to the and the components designed around these values. Light blue indicates that the loop filter will be designed and then the closest value on this list will be chosen.

	***Smart force selected values*** uses the closest known partially integrated filter method and forces the dark teak components and designs the filter. Then it rounds the values to the closest value in the light teal boxes. For this example, C1, C3, C4, R2, R3, and R4 are restricted, but there is no design equations for this case, so the smart force option forces C3, C4, R3, and R4 and designs as normal, but then rounds C1 and R2 to the values on the list.
	***Force selected values*** forces the dark teal values, regardless if there are design equations or not. Be cautions with this approach as it can lead to design failure.
	***Round to listed values*** designs the loop filter as it normally would with no restricted values, but then rounds to the closest value on the list.
	***Ignore these values*** totally ignores these values.

There are only certain combinations of forced combinations allowed that are listed in the table below:

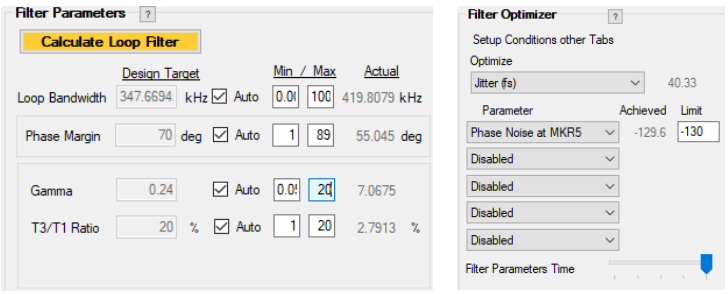
Filter Type	Rules
All Filters	• ***No Forced Components*** is always allowed for any filter order or type • ***All Forced Components*** is always allowed for any filter order or type • ***R3 & C3*** can be forced if it is both components in the case of a 3rd order filter • ***R3, C3, R4, & C4*** be forced if it is all components in the case of a 4th order filter
Active Type A	• ***R1 & C1*** both be forced only for a 2nd order filter with no other components forced • ***R1 or C1*** can be forced for all filter orders if it is not both of them • ***R2 or C2*** can only be forced in a 2nd order when it is not both of them • ***R3, C3, R4, or C4*** can be forced if exactly one or all of these are forced.
Active Type B and C	• ***C1, C2, & R2*** can only be forced in 2nd order filter and only up to one of these. • ***R3, C3, R4, & C4*** can be forced if exactly one or all of these are forced.
Passive	• Any One Component can be forced for any filter order

There are also some things to keep in mind when forcing components:

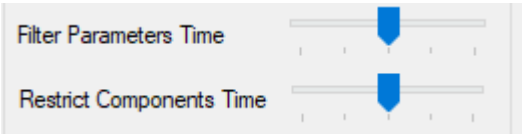
- The smart force option will steer the design towards one of these valid combinations. If the regular force option is used, then the filter designer will return with an error message saying the design is not supported.
- Even in the case that the design is supported, forcing some individual may work for only a narrow range and going out side this range may result in a design failure.
- If the high order capacitor is forced, then the minimum high order capacitance constraint for the loop filter design is ignored.
- The VCO input capacitance can interact with forced components. If one forces the capacitor next to the VCO, then PLLatinum Sim adds the VCO capacitance to that. However, if one forces a different component, then it can distort the results.
    - Consider the case of a 3rd order filter passive filter with R3 forced and the value for C3 for zero VCO input capacitance is 200 pF. Now consider if one modifies this exact same design and makes the VCO input capacitance 100 pF. This will still work and it will just modify C3 to be 100 pF and all other components the same. However, if one modifies the VCO input capacitance above 200 pF, then this will return a valid filter, but the loop bandwidth and other design parameters will be off due to the VCO input capacitance
- In the case the higher order poles are forced (R3 & C3 for 3rd Order filter, R3, R4, C3, & C4 for 4th Order filter), the loop bandwidth may be restricted and the poles T3 and T4 will be restricted by these components. It is also possible to have “degenerate” filter which has C1 = 0 and T1 = 0, but that is still stable.

5.7 The Advanced Optimizer

The advanced optimizer appears in advanced mode when the Optimize box is set to a setting other than “disabled” as shown below. In this case, the user is optimizing the jitter subject to the condition that the phase noise at marker 5 is better than -130 dBc/Hz. These parameters are all taken from the phase noise, spur, and lock time tabs. **The maximum calculation time is limited to the value specified in the Max Calculation Time box on the main diagram.**



When the advanced optimizer enabled, the filter parameters box is updated. And the “Auto Parameter Strategy” combo box disappears as it no longer applies. Instead, PLLatinum Sim iterates using numerical methods for any parameter that has its box checked as Auto. The user can specify Min/Max limits for the optimizer to choose to prevent it from running to an undesired solution.



At the bottom of the filter optimizer group box are Filter Parameters Time and Restrict Components Time (only if there are a list of restricted components). Moving these sliders to the gives the optimizer more power, but takes time. Specifically, here is what the slider is really doing.

Slider Value	Time	Accuracy	Optimization Details
0	Shortest	Minimum	• None
1	…	…	• Sweep BW • Hook-Jeeves parameter sweep, 8 Steps, 12 Iterations
2	…	…	• Sweep BW, ϕ • Hook-Jeeves parameter sweep, 16 Steps, 24 Iterations • Perturb Components 2 steps up/down from design value
3	…	…	• Initial parameter search with ideal NonComponent filter • Sweep BW, ϕ, γ • Hook-Jeeves parameter sweep, 32 Steps, 48 Iterations • Perturb Components 3 steps up/down from design value
4	Longest	Maximum	• Initial parameter search with ideal NonComponent filter • Sweep BW, ϕ, γ • Hook-Jeeves parameter sweep, 64 Steps, 96 Iterations • Perturb Components 4 steps up/down from design value

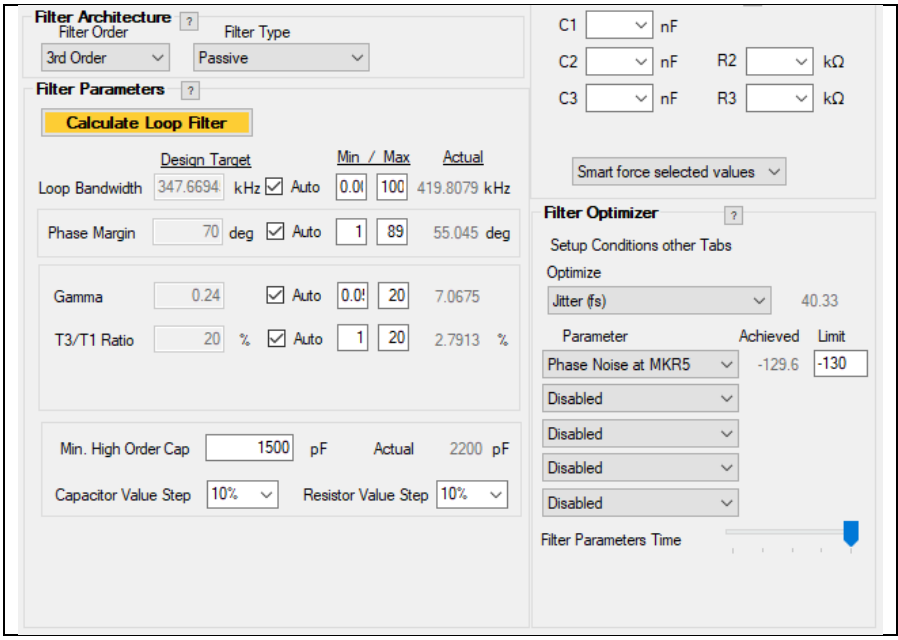
The forced components (dark teal, not the rounded light blue ones) are iterated through according to the following chart.

Slider Value	Time	Accuracy	Optimization Details
0	Shortest	Minimum	Only selected values considered
1	…	…	Up to 3 values and always includes selected value, minimum value, and maximum value
2	…	…	Up to 5 values and always includes selected value, minimum value, and maximum value
3	…	…	Up to 7 values and always includes selected value, minimum value, and maximum value
4	Longest	Maximum	All Values

Tips for the Advanced Optimizer

- Optimizer starts out at specified parameter values. These closer that these are to optimal, the better the optimizer performs
- If optimizer runs out of time, it returns the best solution so far
- For the higher settings, increase the Max. Calculation Time

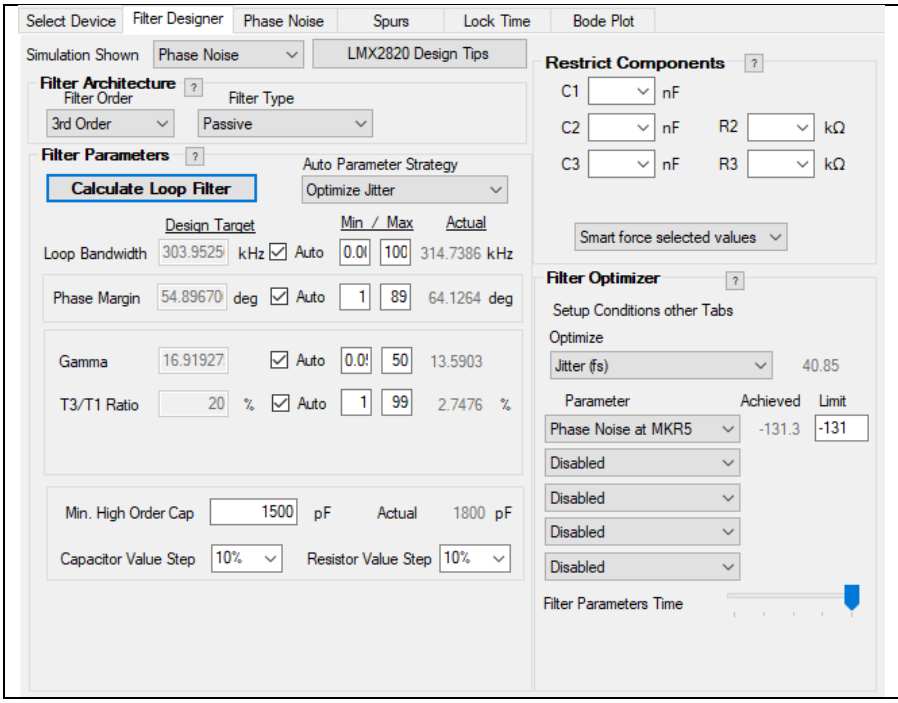
Example Using the Advanced Optimizer



Before Running the Optimizer

The jitter is 40.33 fs and the phase noise at 1 MHz offset (marker 5) is -129.6. dBc/Hz.

This is the same setup using the LMX2820 that has been used in previous figures. The LMX2820 loop filter is fairly well optimized for jitter already, so the impact will not be as much as it would be for a less optimized design. Nevertheless, there is still room for optimization.



After Running the Optimizer

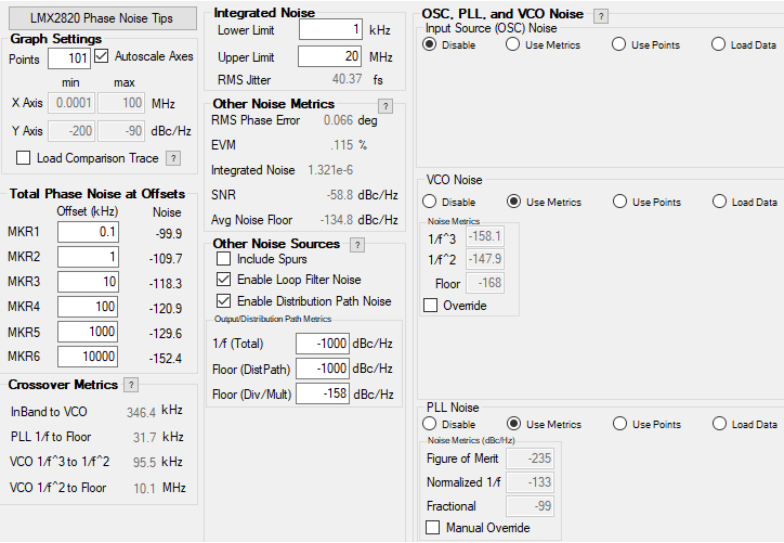
Now impose the constraint that the phase noise at 1 MHz (marker 5) needs to be at least -131 dBc and find the optimal jitter under these conditions.

The max calculation time on the main screen was changed to 300 seconds and the filter parameter time was moved to the last slider position to allow maximum computational power.

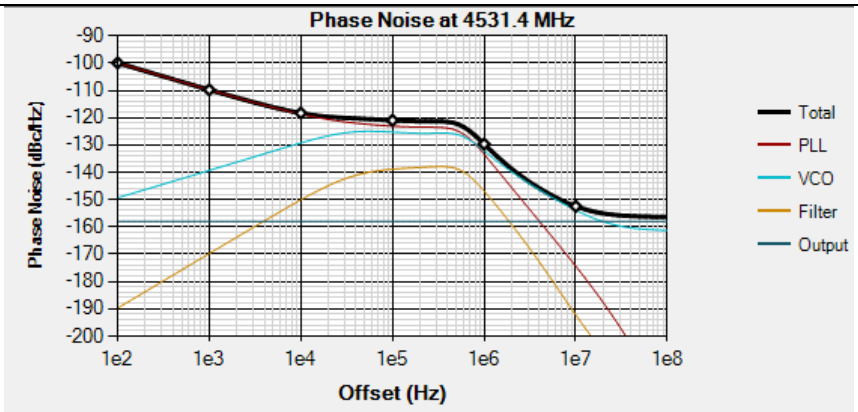
Although the original loop filter was pretty well optimized already, the new filter from the advanced optimizer improves the phase noise at 1 MHz from -129.6 to -131.3 dBc/Hz while increasing the jitter by 0.5 fs.

Phase Noise Tab

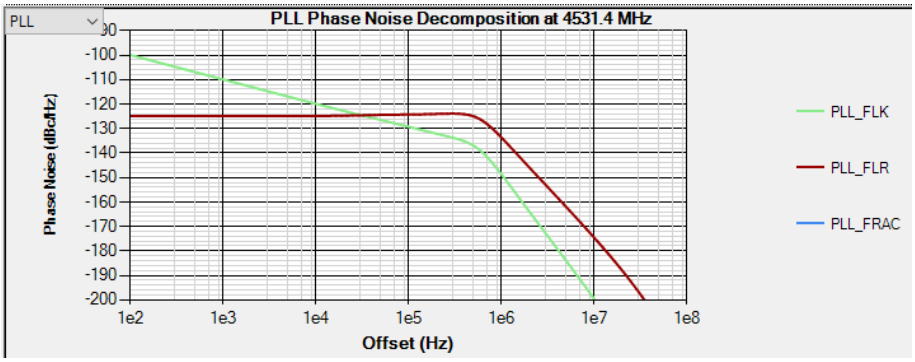
The phase noise tab gives the user to specify phase noise metrics. However, realize that these are read in and calculated from a database and modified automatically based on settings, so it is not necessary to override these metrics in most cases.



The Phase Noise tab gives many options to set up and interpret the phase noise.

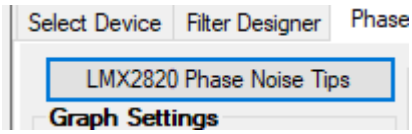


The main phase noise chart appears whenever the Phase noise tab is selected. It can also appear on the filter design tab if it is selected as tie simulation shown. The Total line shows the sum of all sources. It also shows the individual noise sources that add up to the total. One can zoom in and click on this cart to get a closer look

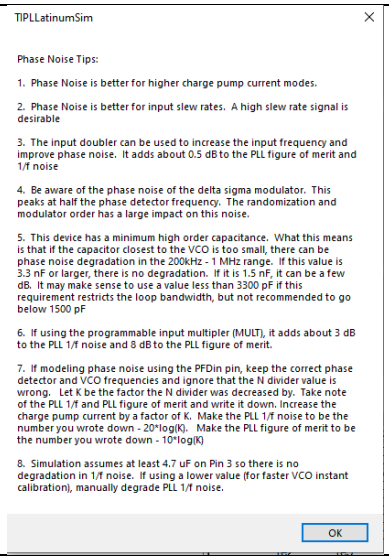


The phase noise decomposition chart appears in advanced mode and allows one to look closer at the OSC, PLL, VCO, Filter, AMP, or Output noise. The noise source of interest can be selected by the combo box in the upper right.

5.8 Phase Noise Tips



Many devices have part specific phase noise tips that are either not modeled or need special modifications for modeling. Be sure to click the phase noise tips button to see all the details.



5.9 Loading Phase Noise Traces

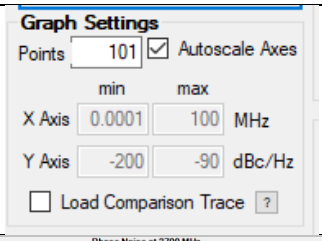
5.9.1 General Method of Loading Phase Noise Traces

The phase noise tab allows the user to load a comparison trace, OSCin phase noise trace, PLL phase noise trace, or VCO phase noise trace. These are under different sections, but the general file format is:

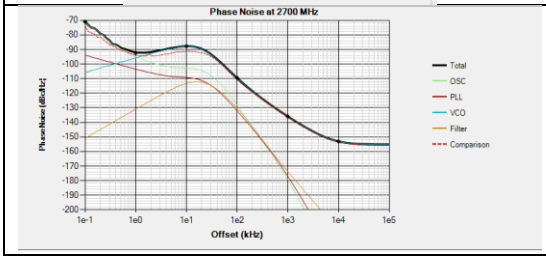
<Offset in Hz> + <Tab> +<Phase Noise>+ <Carriage Return>

Comma or space can also be used in place of the <tab> and any entry with an # is ignored and can be used for comments. If using excel, simply use a the first column for offset and the second one for phase noise and save as tab delimited text.
The frequency is assumed to be whatever is specified on the main diagram.

5.10 Graph Settings & Comparison Trace

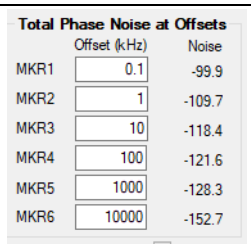


- Points are used in the graph and having a very large number of points may increase computational time as this is used for numerical integration. The X Axis and Y axis should be self-explanatory.
-



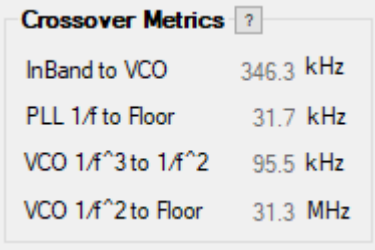
The comparison trace allows the user to load a trace to compare to the actual one. The most common use is to load in actual measured data so that it can be compared directly to the simulation. This is using the LMX2581 EVM with on board XO. Note the red (comparison) and black (Total) traces are I good agreement.

5.11 Total Phase Noise at Offsets



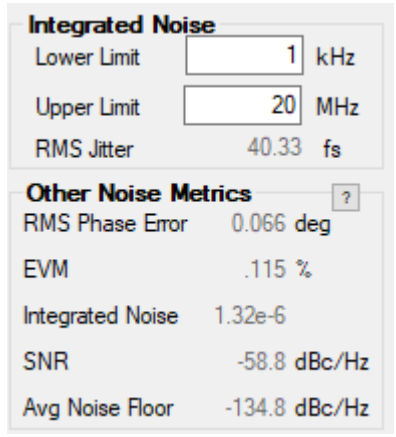
- Points are used in the graph and having a very large number of points may increase computational time as this is used for numerical integration. The X Axis and Y axis should be self-explanatory.
- The comparison trace allows the user to load a trace to compare to the actual one. The most common use is to load in actual measured data so that it can be compared directly to the simulation

5.12 Crossover Metrics



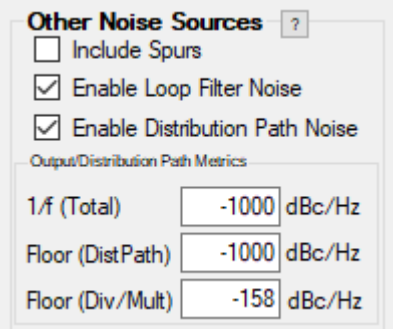
PLLatinum Sim models OSC, PLL, and VCO phase noise using flat, 1/f, $1/f^2$, and $1/f^3$ curves. These metrics show where these regions cross.

5.13 Integrated Noise and Other Noise Metrics



- The integrated noise is calculated using the specified Lower and Upper Limit values.
- The RMS Jitter is what the filter optimizer references
- Other interpretations of integrated noise floor are also shown as calculated from the phase noise

5.14 Other Noise Sources



- Include Spurs checkbox displays the spurs and adds their energy to the integrated noise metrics
- Enable Loop Filter Noise enables the noise of the resistors in the loop filter as well as the noise of the op-amp if an active filter is used
- Enable Distribution Path Noise enables the noise of the output buffer as well as any multipliers or dividers. Note that for some devices, the output buffer noise is included in the VCO where as in others, it is separated out

5.15 OSC, PLL, and VCO Noise

5.15.1 Disable Option

When the option is set to Disable, the noise source is disregarded.

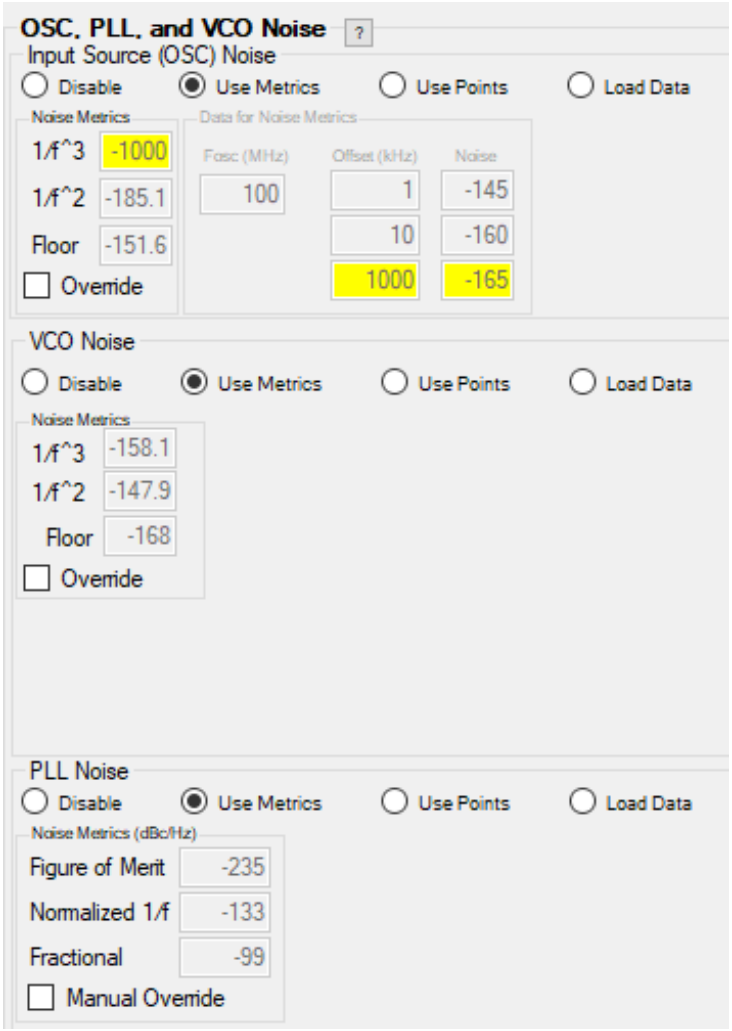
5.15.2 Use Metrics Option

OSC and VCO Noise Metrics

The OSC and VCO noise are modeled as the sum of 1/f^3, 1/f^2, and Floor metrics. These metrics are normalized to 1 GHz carrier and 1 MHz offset. The 1/f^3 and 1/f^2 noise are assumed to vary as 20*log(frequency) and the floor is assumed to vary as 10*log(frequency). They can either be manually entered or calculated by specifying three phase noise offsets. Ideally one offset should be mainly on the 1/f^3 slope, another on the 1/f^2 slope, and the third on the noise floor. PLLatinum Sim tries to solve this using three equations and three unknowns, but if one provides two points on the slope, one of them will be ignored and the noise will be modeled with less than three noise slopes. When the offsets are specified, be sure to push the button to update the VCO or PLL metrics. For the VCO metrics, there is the option to use a two-frequency model in the case that the metrics vary significantly between the minimum and maximum VCO frequency. For any VCO frequency in between, a linear interpolation is used

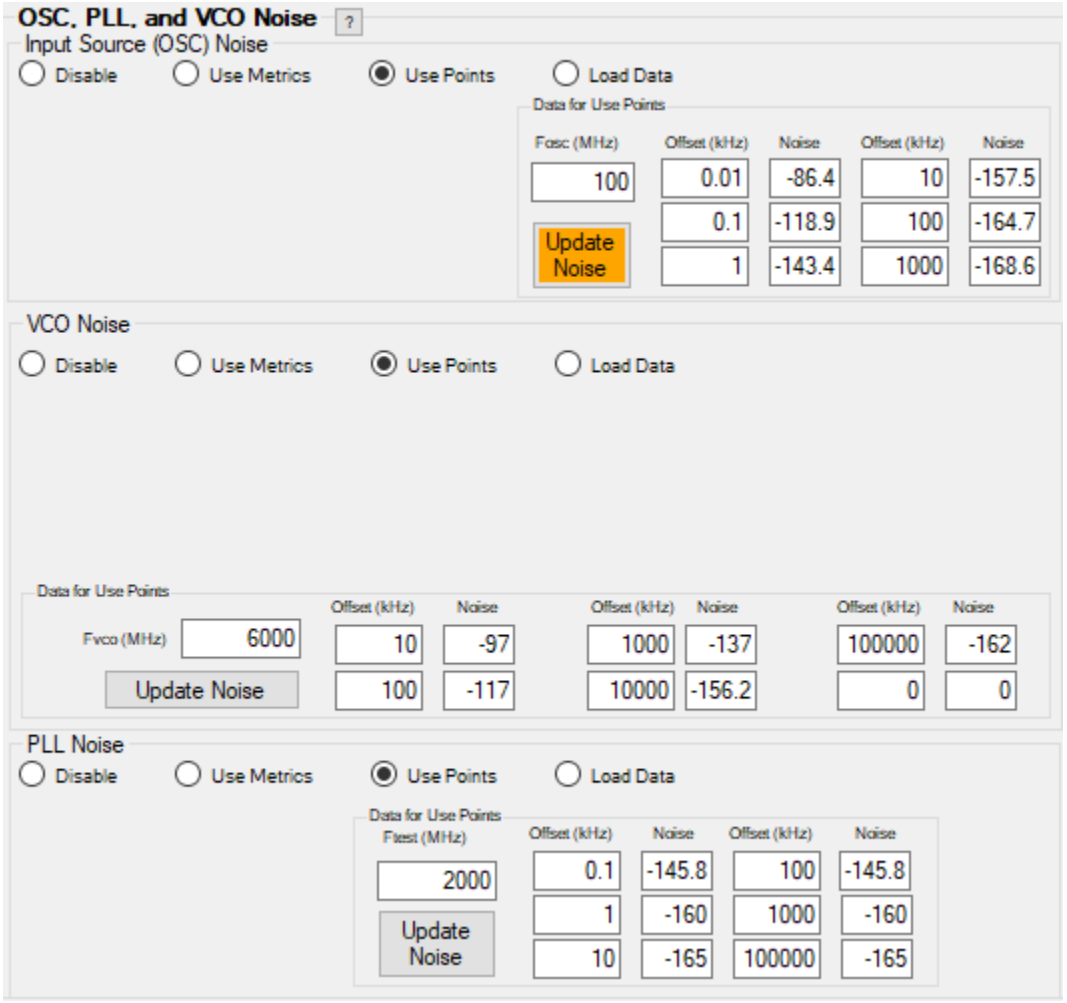
PLL Noise Metrics

For the PLL noise, the PLL figure of merit, the normalized 1/f noise (1 GHz carrier, 10 kHz offset), and the fractional PLL noise.



5.15.3 Use Points Option

Up to six points can be specified and points in between will be estimated. If less than six points are used, put "0" for the offset. Once these are entered, press the "Update Noise" for this to actually be applied.

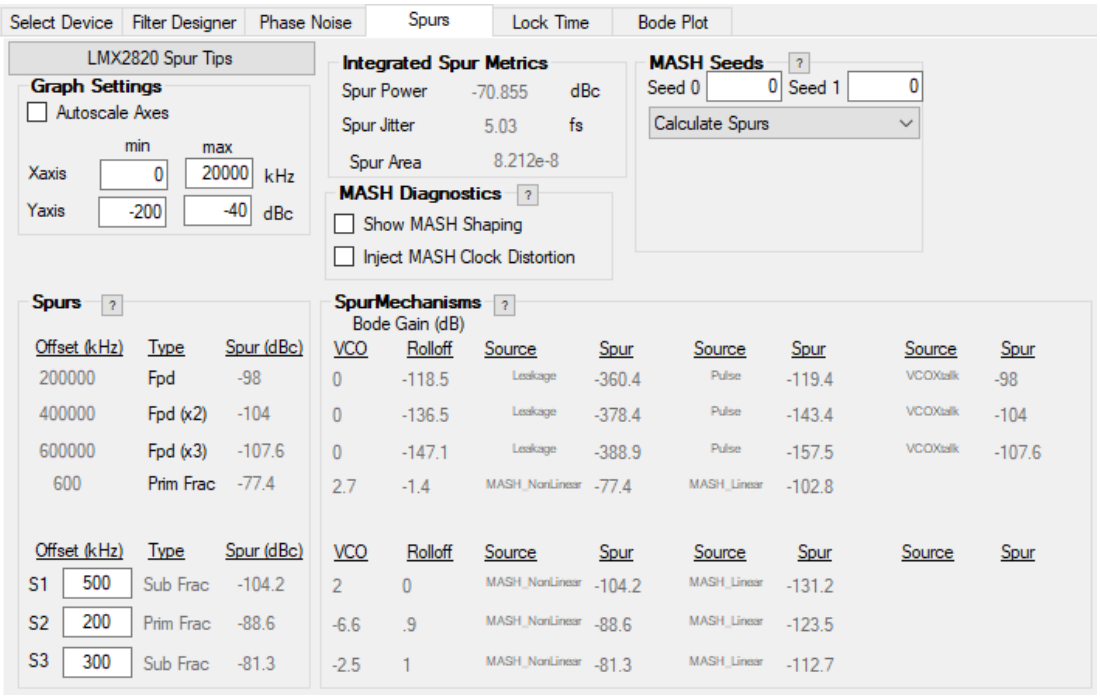


Load Trace Option

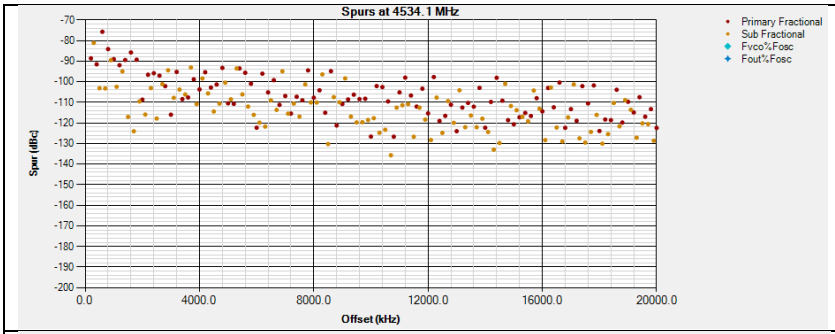
A phase noise trace can be loaded using the method previously stated.

6 Spurs Tab

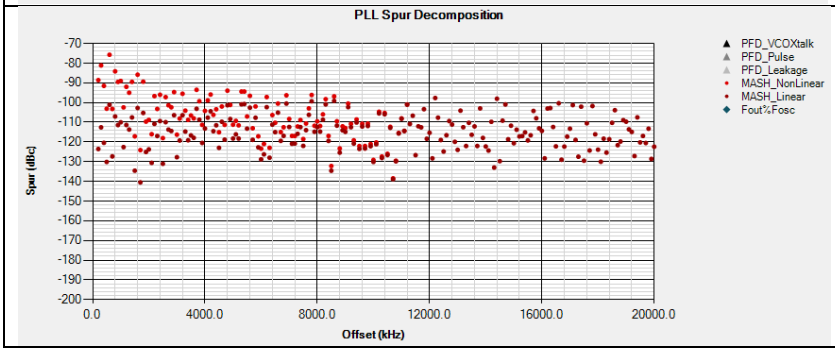
The spurs tab gives detailed modeling of spurs including integer spurs, fractional spurs, and spurs due to crosstalk on the chip. Note that the fourth entry in the "Spurs" section is the highest spur that is not mentioned anywhere else and within the graph settings range. Spur simulations do not always perfectly match measured results and do not account setup conditions, process/temperature variations, layout, and many other factors. That being said, the spur simulator gives good insight as to where the spurs occur and some of the most common contributors to them.



6.1 Spur Chart and Decomposition Chart

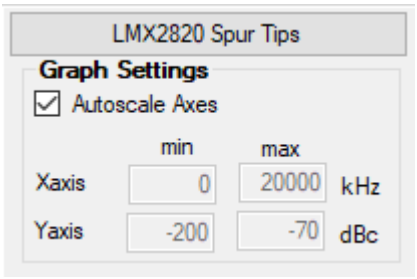


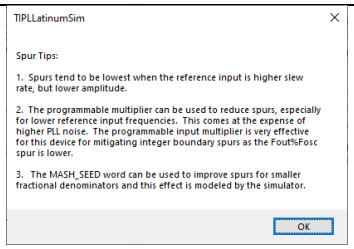
The main spur chart shows the spurs at various offsets. One can mouse over spurs and zoom in on this graph. For intuitive understanding with fractional spurs, it is sometimes useful to move the randomizaton Slider or MASH Order settings on the main diagram to visually see the impact.



The spur decomposition chart appears in advanced feature level and shows each spur contributor at each offset instead of the total spur.

6.2 Spur Tips and Graph Settings

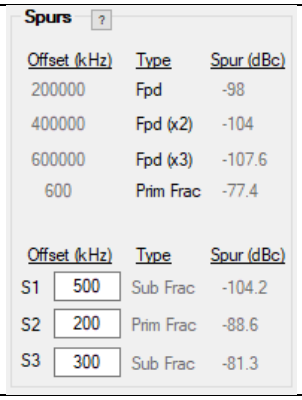




The spur tips button shows part specific spur hints when clicked.

For the graph settings, one thing to keep in mind is that if one is doing fractional spurs, increasing the X axis has a dramatic impact on calculation time for fractional spurs. If this time exceeds Max Calculation Time on the Main Diagram, then the calculation will stop. In summary, if simulating in fractional mode with many small fractional spurs, do not set the max Xaxis to be orders of magnitude larger than needed.

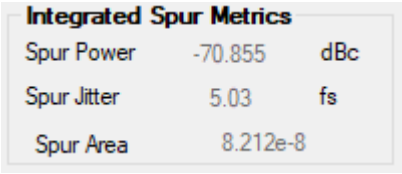
6.3 Spurs Box



The top half of the box shows the first three phase detector spurs and if fractional mode is used then the integer boundary spur (IBS) and primary fractional spur as well.
Below that are three entry boxes where an offset can be chosen and then PLLatinum Sim will try to find the closes spur to this specified offset.
All the spur types are

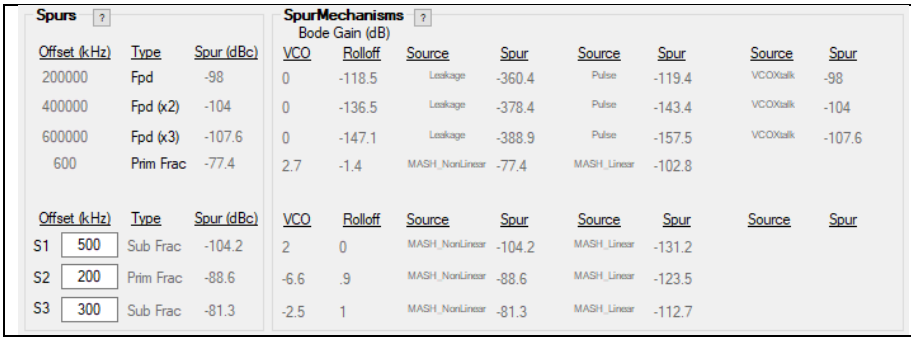
Be sure to click on the "?" icon for more information about the spur types.

6.4 Integrated Spur Metrics



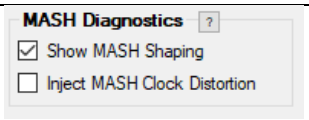
Integrated Spur Metrics are calculated by integrating the spur power. The integration range is the range specified for the "Xaxis" on the graph settings on the spur tab. Be aware that on the Phase Noise tab, the integration range is different and this range on the spur tab also applies to spur energy calculated on the Phase Noise tab.

6.5 Spur Mechanisms

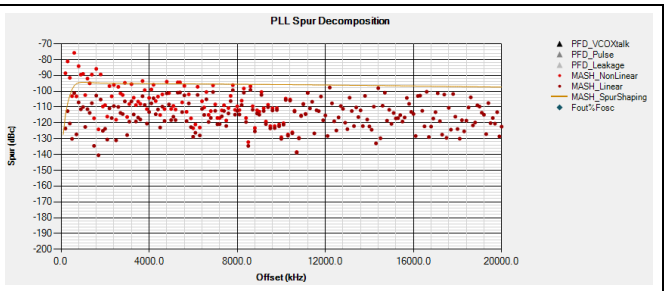


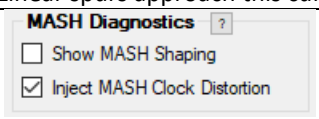
Spur Mechanisms gives an idea of what mechanisms are contributing to each spur. Be sure to click on the "?" icon in spur mechanisms to get detailed descriptions of what each of these mechanisms are.

6.6 Spur Diagnostics

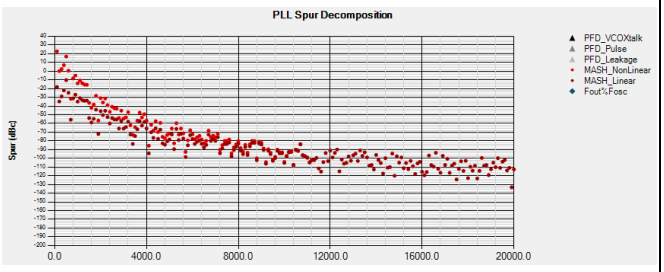


When ***Show MASH Shaping*** is selected, the MASH_Spur Shaping trace appears on the Spur Decomposition chart. As the randomization approaches 100%, the MASH_Linear spurs approach this curve.



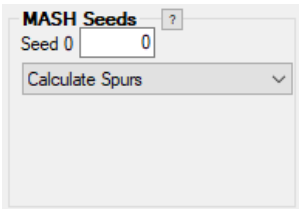
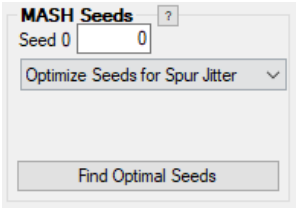
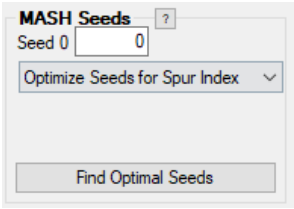
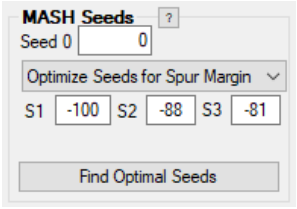


Inject MASH Clock Distortion exaggerates the impact of the uneven clock coming from the N divider by assuming the VCO frequency does not move. It us a diagnostic tool to see which spurs are impacted by lower N divider values. ***This does not represent actual spur levels.***



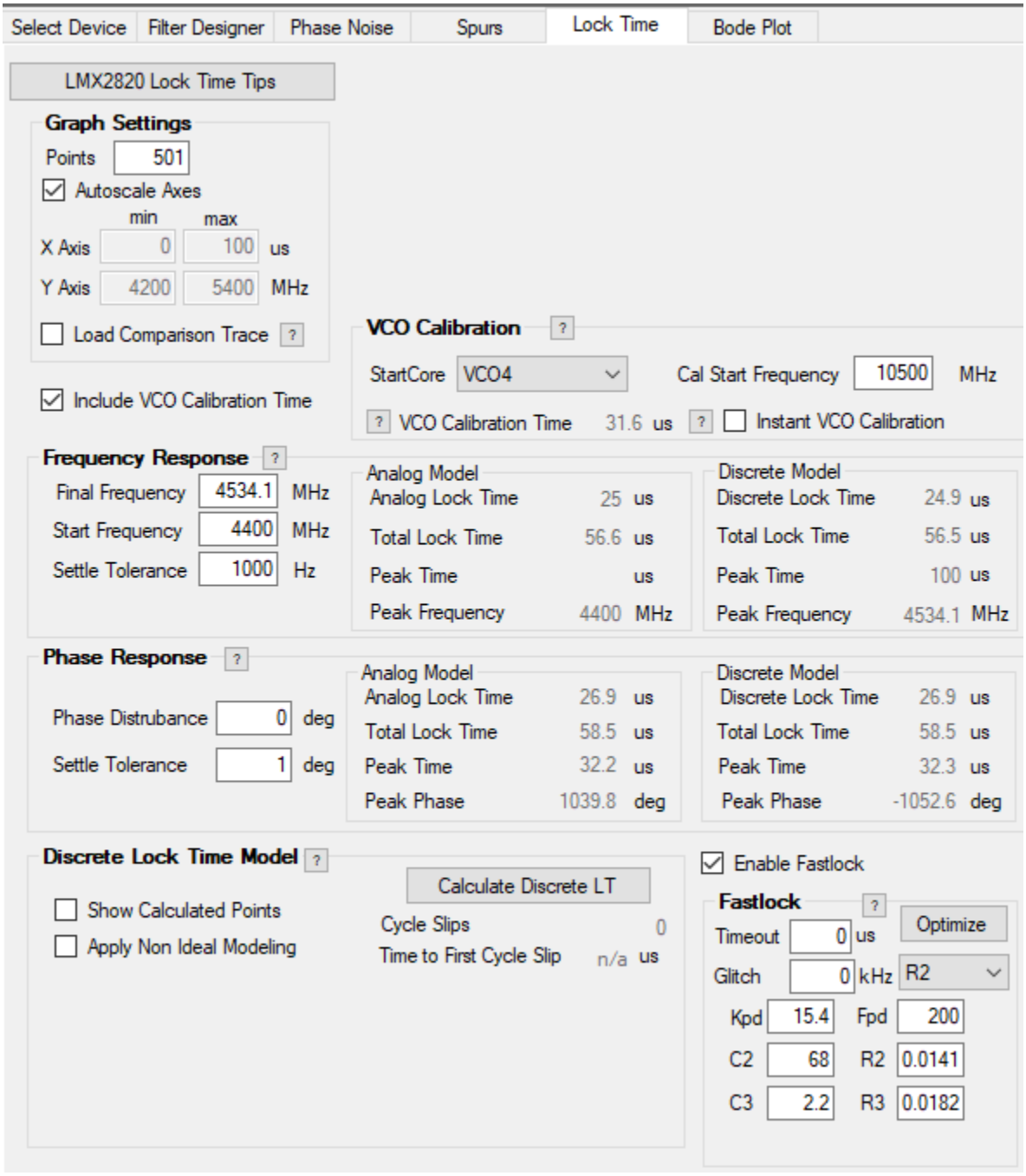
6.7 MASH Seeds

MASH seeds impact the initial starting values and numerical sequence of the MASH engine, thus impacting fractional spurs. They can be used to optimize spurs for smaller denominators (say <=1000). Also, they can shift phase and cause unwanted spurs. PLLatinum Sim models their impact.

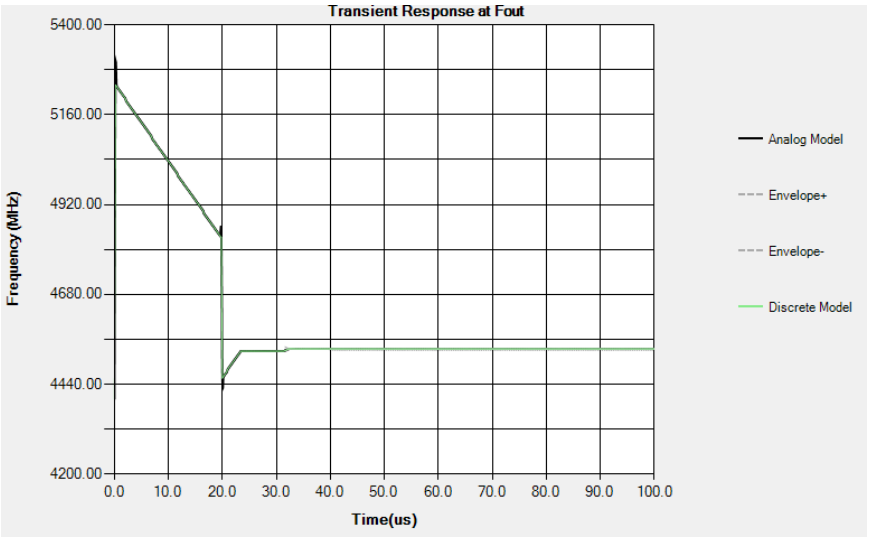
	***Calculate Spurs*** finds the spur levels with the given seed values.
	***Optimize Seeds for Spur Jitter*** searches through the seeds to find the values that minimize the spur jitter in the integrated spur metrics group.
	***Optimize Seeds for Spur Index*** searches through the seeds to find the values that minimize 3*S1+2*S2+S3. S1, S2, and S3 are specified in the Spurs group box.
	***Optimize Seeds for Spur Margin*** searches for the spurs that gives the most margin. It compares the S1, S2, and S3 spurs in the spur group to the S1, S2, and S3 design targets in the MASH Seeds group and tries to maximize the margin for the worst case spur.

7 Lock Time Tab

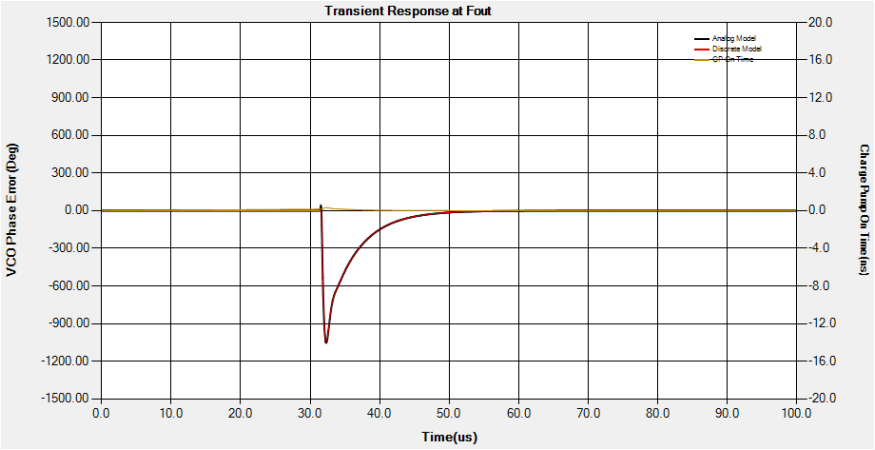
The lock time tab gives the ability to model the lock time. This includes VCO digital calibration time, lock time to frequency, lock time to phase, and a discrete lock time model that accounts for the discrete sampling action of the phase detector and nonlinearity of the charge pump. Due to longer potential computation times, the discrete model is only calculated when the "Calculate Discrete LT" button is pressed.



7.1 Lock Time Frequency and Phase Chart

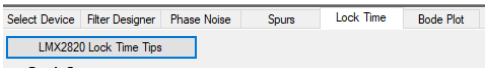


The lock time chart shows the frequency vs. time. The default is to use the analog model (continuous time approximation for the charge pump). The exponential envelopes are calculated.

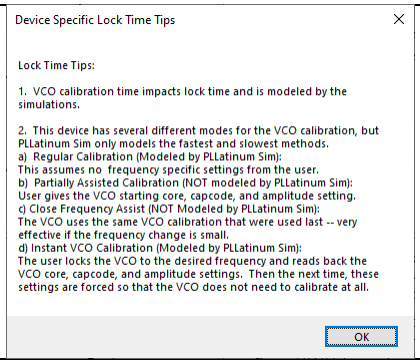


The secondary lock time chart appears in advanced feature level and shows he phase error vs. time.

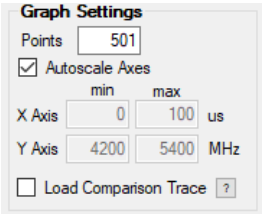
7.2 Lock Time Tips



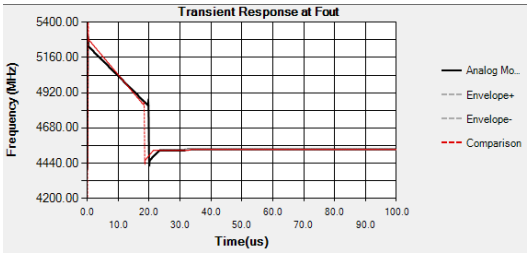
Many devices have part specific lock time tips that are either not modeled or need special modifications for modeling. Be sure to click the lock time tips button to see all the details.



7.3 Graph Settings and Comparison Trace



The graph settings are self-explanatory.

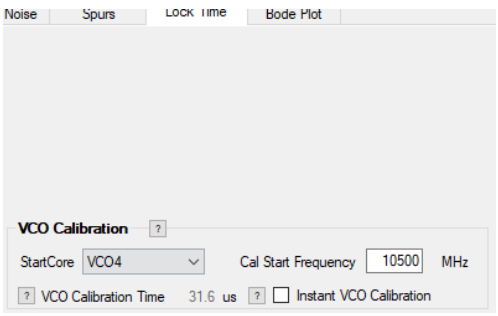


There is the option to load a comparison trace. The input format to this is:

<Time in Seconds> + Tab + <Frequency in Hz> + <Carriage Return>

The black trace is the simulated value where the red trace is the actual measurement.

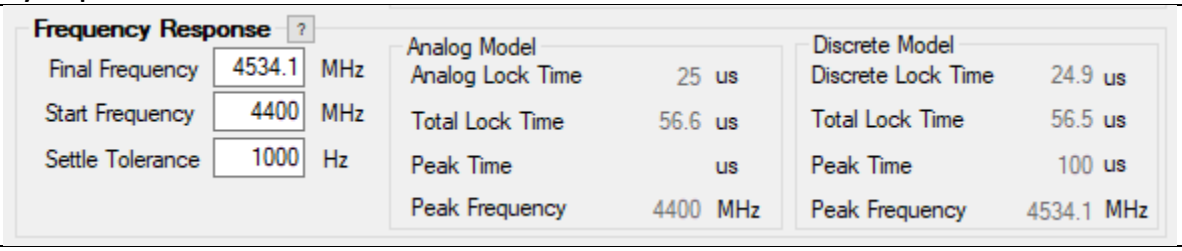
7.4 VCO Calibration Time



For devices with integrated VCO, the calibration time can also be modeled. Often there is a special speed-up mode that goes by different names (Called “Instant VCO Calibration”) for this device. Click the “?” for device specific information on this feature.

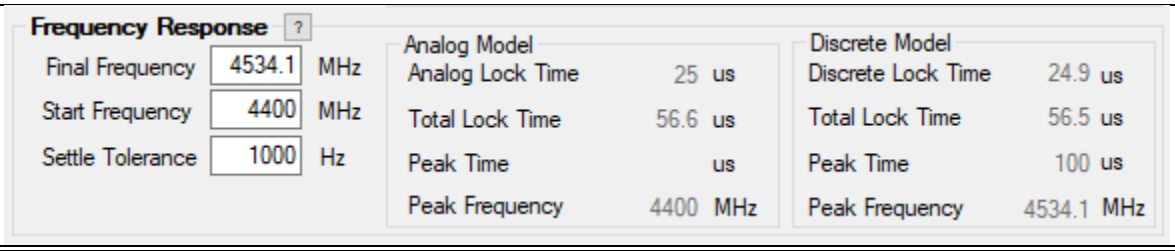
The VCO Calibration Start group allows the user to specify the starting core and frequency. Depending on the device and choice for the special speed up mode this box will be labeled “Cal Start Frequency” or “Cal Assist Error”.

Frequency Response Box



The frequency reponse box models the frequency response. The start and final frequencieshave restrictions and get automatically updated based on these. The start and final frequencies have to use the same output divider, the Cal Start freuqency updates the start frequency for some devices with VCO calibration, and the start and final frequencies cannot be outside the VCO range (including dividers/multipliers). The Analog Model assumes poles and zeros of the loop filter and uses the continuous time approximation to model the charge pump. The Discrete Model can be enabled to model the discrete modeling action of the phase detector.

7.5 Phase Response Box

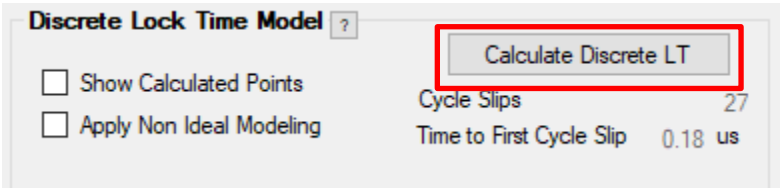


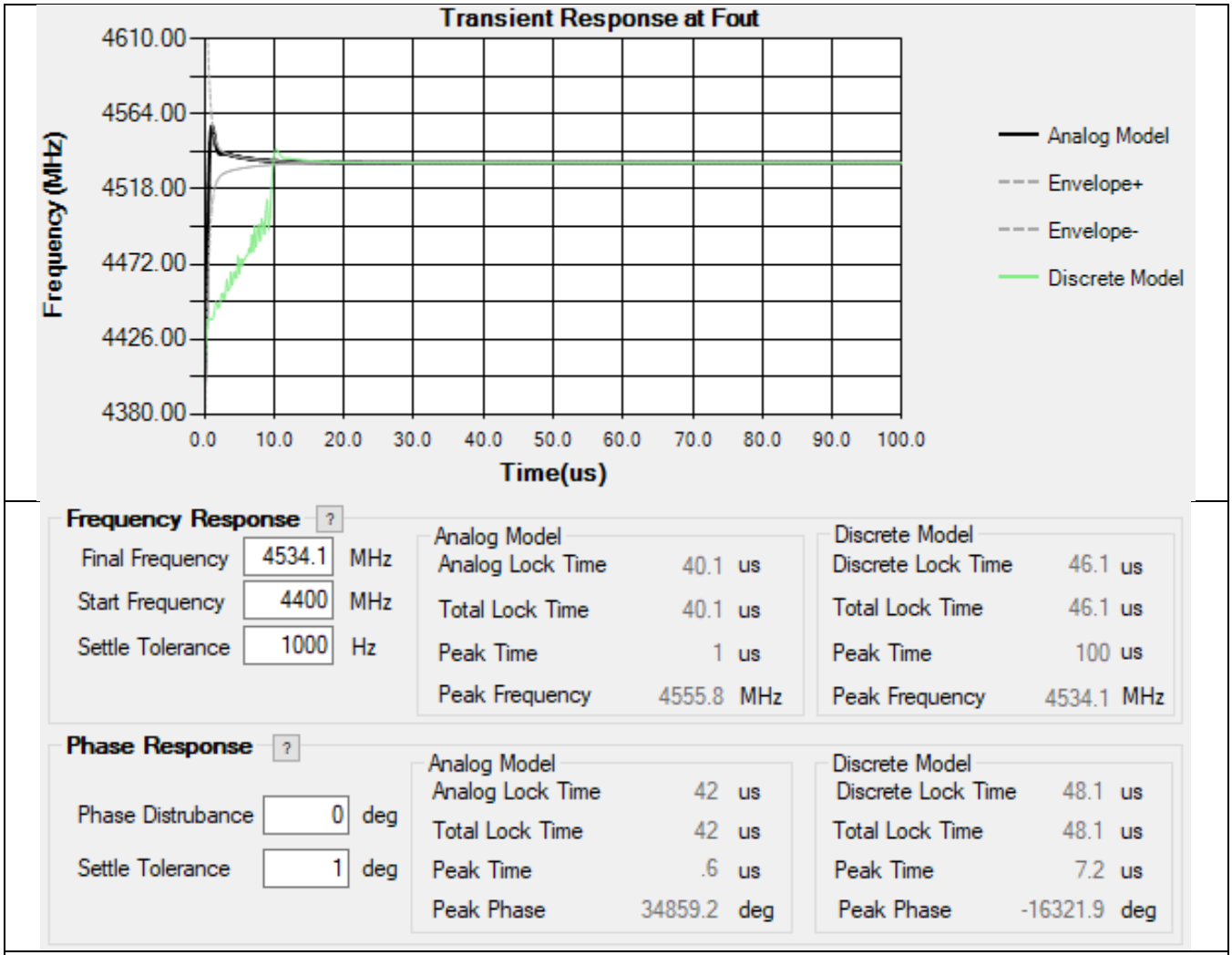
The phase response box models the phase of the output and lock time to a phase. A nonzero entry for the Phase Disturbance can be given to model a step response in phase and this is shown in the graph on the lower left.

7.6 Discrete Time Modeling of Lock Time

The discrete lock time modeling calculates the lock time by calculating the frequencies, phases, and loop filter voltages at every cycle of the charge pump. It is run whenever the "Calculate Discrete LT" button is pushed. Some things to keep in mind.

- The discrete lock time model works after the VCO calibration is finished. For the examples in this section, the VCO calibration was disabled to make the impact of the discrete lock time modeling more obvious.
- The discrete lock time model only calculates when "Calculate Discrete LT" button is pushed
- If the calculation takes longer than Max Calculation Time on the Main Diagram, it truncates the X axis time.

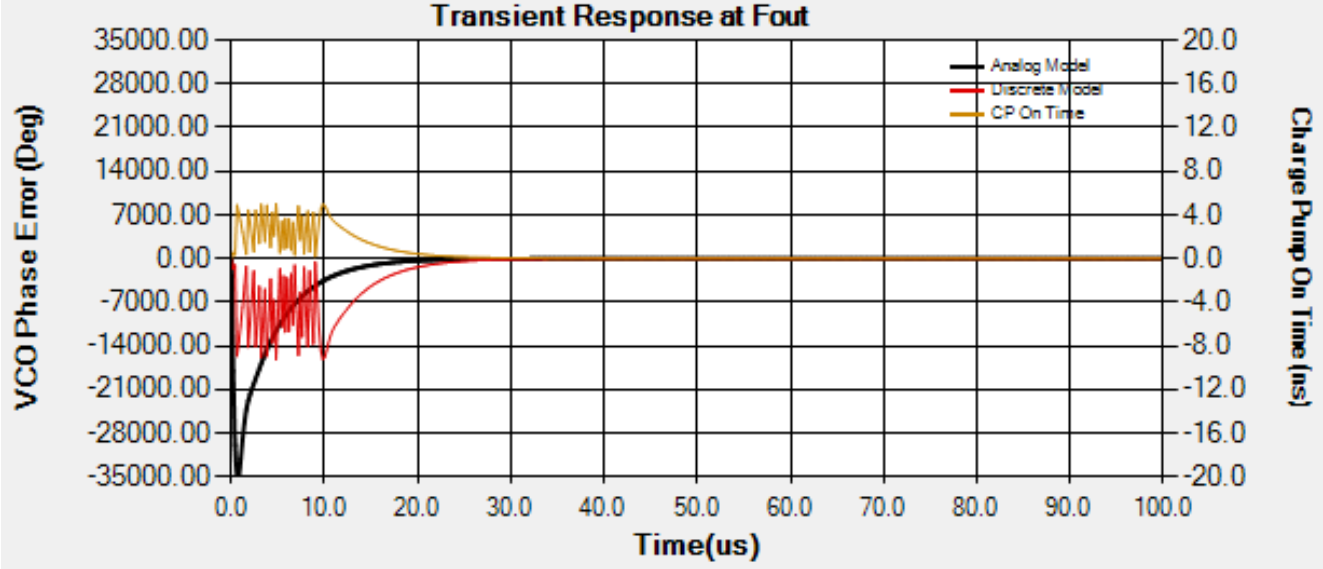




Comparing the discrete model to the analog model, we see that it shows the true transient response is slower due to the cycle slipping caused by the discrete sampling action of the phase detector.

7.6.1 Transient Phase Response for Discrete Modeling of Lock Time

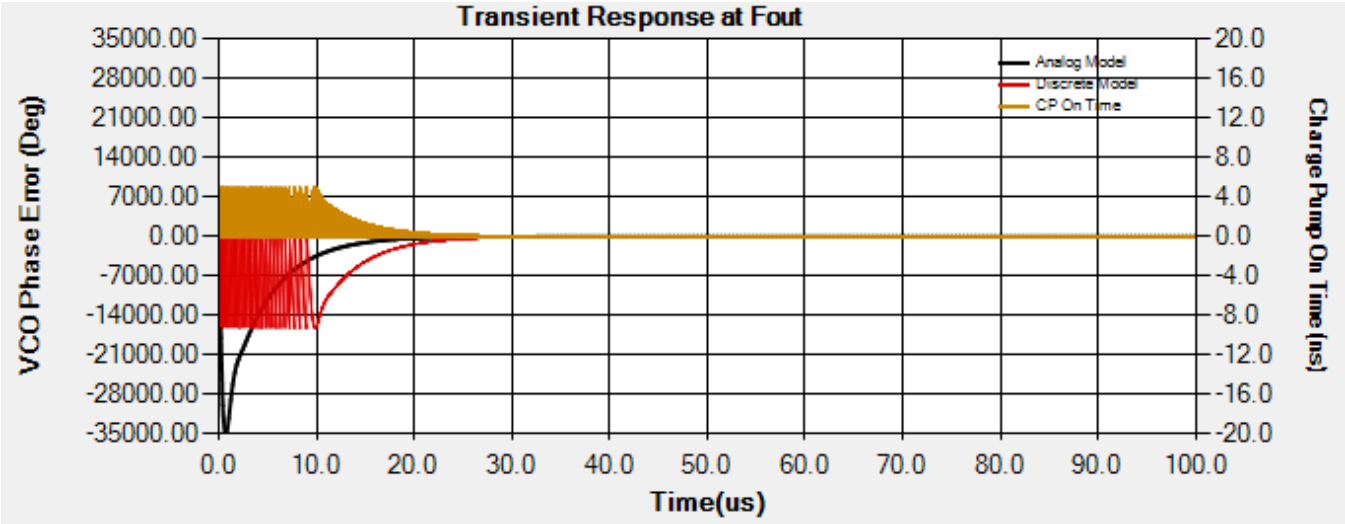
☐ Show Calculated Points



When lock time is modeled in a discrete way, the secondary lock time graph shows some additional information. It compares the analog and discrete modeling of the phase error. If the frequency change is small, then these graphs match at least a little. But if there is a large frequency change (relative to the loop bandwidth), then cycle slipping can occur and the discrete model shows a larger phase error and the graph may not show state phase error (although the actual PLL does settle to zero steady state phase. The charge pump on time shows how long the charge pump comes on. A negative time indicates that the charge pump is pumping in the negative direction. So a -8 ns charge pump on time means that the charge pump is sinking current for 8 ns.

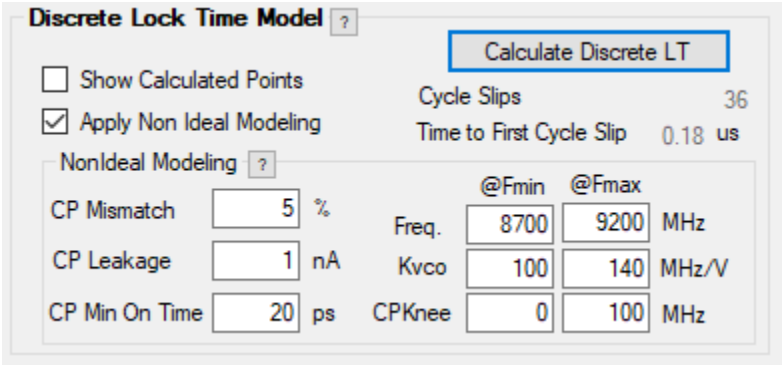
Clicking the "Show All Points" option is useful if one is interested in the charge pump on time. Often times, the number of points is too small to show all the interesting behavior, but checking this option calculates at every charge pump event to really show all the detail. ***However, it ,may take much longer to calculate.***

☑ Show Calculated Points



7.6.2 Nonlinear Modeling of the Charge Pump

This is using the same example as before except now adding additional parameters for nonlinear modeling. One can enter a "0" in any of the fields to have it not impact calculations.



Charge Pump Mismatch, Leakage, and Minimum On Time

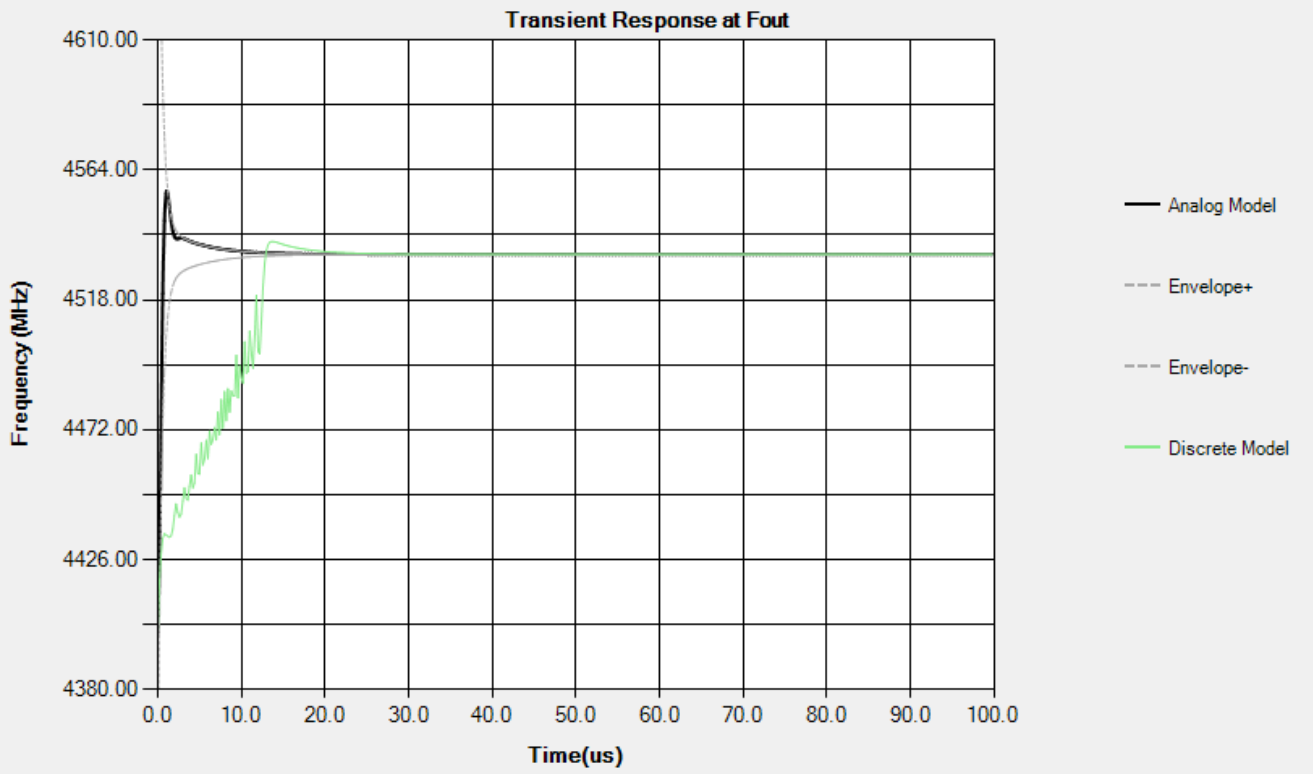
- ***CP Mismatch*** is the amount that the positive charge pump current is greater than the negative charge pump current
- ***CP Leakage*** is the amount of leakage current that occurs when the charge pump is off
- ***CP Min On Time*** is the minimum charge pump on tome
- ***CP On Time Low*** is calculated on time for the last time the charge pump was sinking current.
- ***CP On Time High*** is calculated on time for the last time the charge pump was sourcing current.

Modeling @Fmin and @Fmax

- ***Freq.*** specifies the minimum and maximum frequencies that apply to the two boxes below
- ***Kvco*** is the VCO gain at the above minimum and maximum VCO frequencies
- ***CPKnee*** is the knee for the charge pump and models the effect of the charge pump current being reduced when the tuning voltage is near the rails of the charge pump. CPKnee of "0" means disregard and CPKnee cannot be negative.
  - $Sink\ Current = -Kpd \cdot \left(1 - \exp\left(\frac{Fvco - Freq@Fmin}{CPKnee@Fmax}\right)\right)$
  - $Source\ Current = Kpd \cdot \left(1 - \exp\left(\frac{Freq@Fmax - Fvco}{CPKnee@Fmin}\right)\right)$

Here is how the Kvco and charge pump current would be calculated for the above example.

Frequency (MHz)	Kvco (MHz/V)	Sink Current	Source Current		Settings
8700	84.2	0	*Kpd*		Fmin = 8700 MHz
8800	98.2	-0.632· *Kpd*	*Kpd*		Fmax = 9200 MHz
8900	112.2	-0.865· *Kpd*	*Kpd*		CPKnee@Fmin = 0 MHz
9000	126.2	-0.950· *Kpd*	*Kpd*		CPKnee@Fmax = 100 MHz
9068.2	135.7	-0.975· *Kpd*	*Kpd*		Kvco@Fmin = 84.2 MHz
9100	140.2	-0.982· *Kpd*	*Kpd*		Kvco@Fmax = 154.2 MHz
9200	154.2	-0.993· *Kpd*	*Kpd*		



Frequency Response

Final Frequency	4534.1	MHz
Start Frequency	4400	MHz
Settle Tolerance	1000	Hz

Analog Model		
Analog Lock Time	40.1	us
Total Lock Time	40.1	us
Peak Time	1	us
Peak Frequency	4555.8	MHz

Discrete Model		
Discrete Lock Time	46.4	us
Total Lock Time	46.4	us
Peak Time	100	us
Peak Frequency	4534.1	MHz

Phase Response

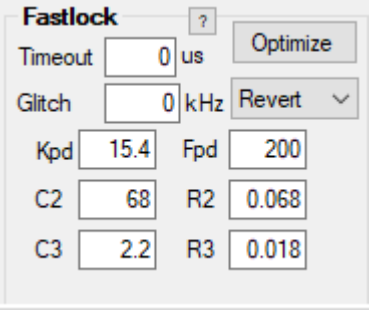
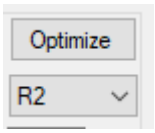
Phase Distrubance	0	deg
Settle Tolerance	1	deg

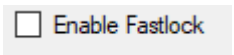
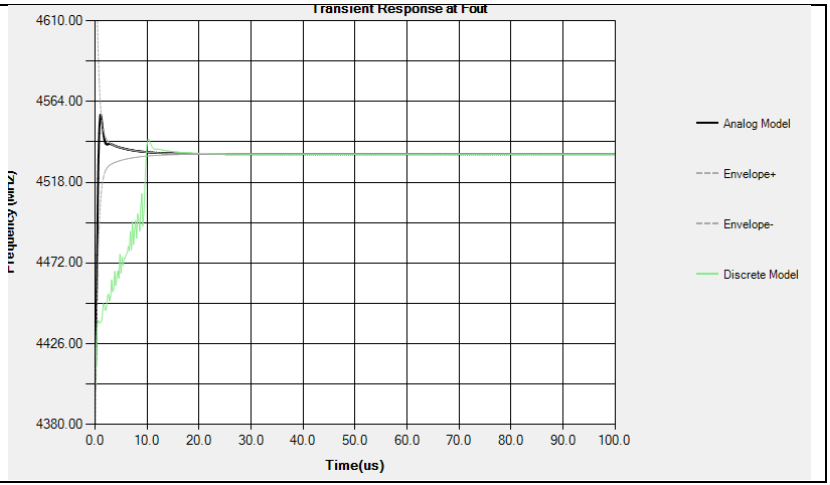
Analog Model		
Analog Lock Time	42	us
Total Lock Time	42	us
Peak Time	.6	us
Peak Phase	34859.2	deg

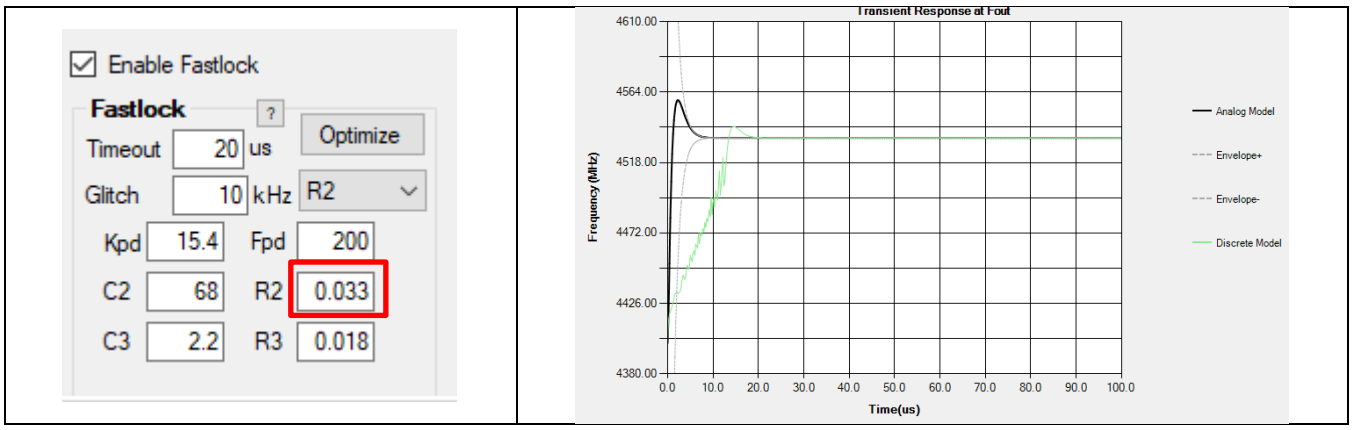
Discrete Model		
Discrete Lock Time	39.9	us
Total Lock Time	39.9	us
Peak Time	1	us
Peak Phase	-16288.8	deg

Comparing this to the example without the nonlinear modeling, we see that the lock time is slightly different

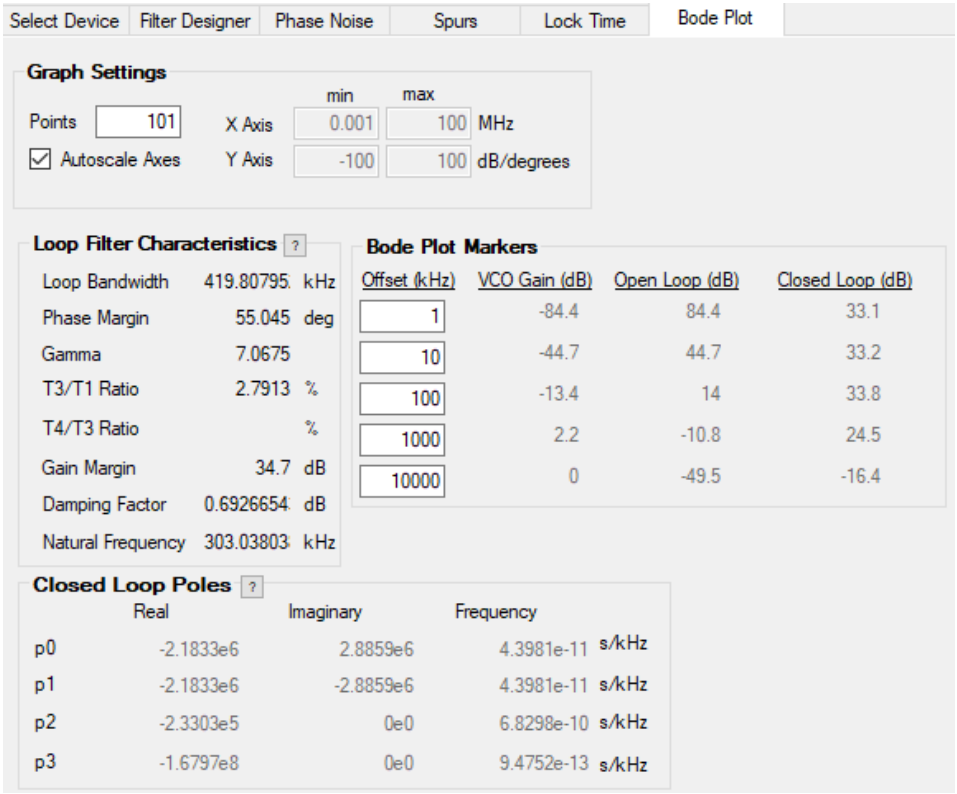
7.7 Fastlock

	Fastlock refers to switching in a faster switching loop filter initially when the analog lock time begins (after VCO frequency calibration) and then switching it out after a certain amount of time. **Note:** Although PLLatinum Sim may show Fastlock, this does not imply that the device has timeout counters, switches, and changeable charge pump gain to support Fastlock. In other words, external circuitry would be required if not integrated on the PLL IC itself.
	**Fastlock Settings** • ***Timeout*** is how long fastlock is engaged before it is switched out. • ***Glitch*** is assumed glitch that occurs when fastlock is switched out. • ***Kpd*** is the effective charge pump current during fastlock. • ***Fpd*** is the effective phase detector frequency during fastlock. • ***C2, C3, C4, R2, R3, R4*** are the effective loop filter values during fastlock. Note: If one does NOT want the fastlock timeout count to be automatically applied and show when the disctete model is calculated, ensure that the combination box is selected to anything but “Timeout”
	**Fastlock Component Optimizer** Pressing the Optimize button optimizes the component values to minimize lock time during fastlock. It has a few different options what to optimize • ***Timeout*** optimizes analog timeout count when the “Optimize” button is pushed. If discrete model is run with this option chosen and a nonzero option for the timeout count, it updates it for the optimal discrete model timeout count. • ***R2*** optimizes only the effective value of R2 • ***C2*** optimizes only the effective value of C2 • ***C3, C4, R2, R3, R4*** optimizes these components. • ***All but C1*** optimizes all components except C1. • ***Revert*** changes all component values back to the ones on the main diagram.

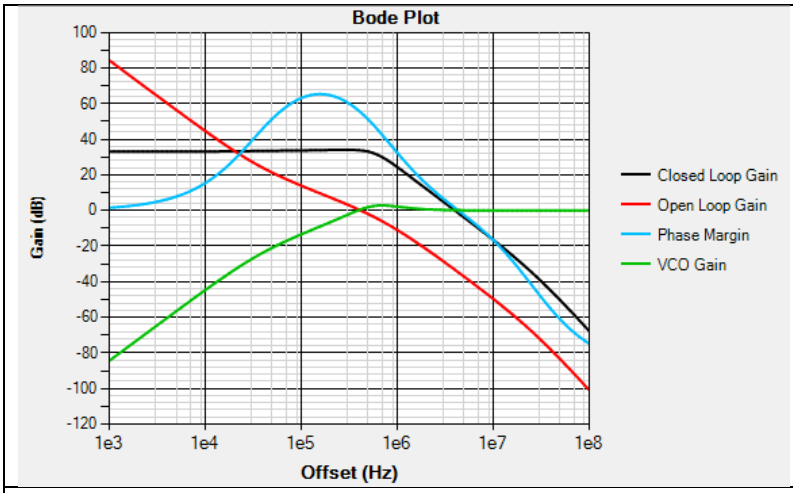
	



8 Bode Plot Tab



8.1 Graph and Poles and Time Constants



The graph is similar to the others and the user can zoom in and see it interactively change

Poles and Time Constants

	Design Target	Actual			Design Target	Actual	
T2	4.7303e-6	4.6308e-6	s	T2	3.3646e1	3.4369e1	kHz
T1	7.8283e-8	2.134e-7	s	T1	2.0331e3	7.4581e2	kHz
T3	1.5657e-8	5.9566e-9	s	T3	1.0165e4	2.6719e4	kHz
T4	0	0	s	T4	n/a	n/a	kHz
A0	3.0816e-7	7.074e-8	F				
A1	2.8949e-14	1.5517e-14	sF				
A2	3.777e-22	8.9919e-23	s^2*F				
A3	0	0	s^3*F				

The poles and time constants show the values. Note that the design target and actual values can be different due to component rounding, VCO input capacitance, and a minimum high order capacitor requirement in the filter design. If there are 0's in the design target, it indicates the filter has not been designed.