

CLOCK-PERFDATA-DESIGN

Clock performance data and register settings for clock generators, network synchronizers, jitter cleaners, and other clocking devices.

Release Notes



Rev. 2025-01-30
30-Jan-2025

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Release Notes

CLOCK-PERFDATA-DESIGN

Release 2025-01-30

1 Overview

This document is the Release Notes of the CLOCK-PERFDATA-DESIGN site. This release gives list of features/known issues of every release.

2 Licensing

Please refer to the software manifest which outlines the licensing status for all packages included in this release.

3 Documentation

- **.tcs files:** Provides the TICS Pro v1.7.7.6 configuration file for the setup.
- **.txt files:** Provides the raw output phase noise data exported from the Keysight E5052A or E5052B phase noise analyzer.
- **.png files:** Provides the output phase noise plot capture or setup diagram. Refer to the file name for content detail.

4 Device Support

The devices supported with this release include (new devices are bolded):

Supported Devices
LMK5C33414A
LMK5C33216A
LMK5B33216

5 Supported Features

5.1 Version 2025-01-30

- Added Configuration Files and Data
 - LMK5B33216
 - LMK5B33216_ConfigAndData_REF_is_None_XO_is_48MHzSMA100B_OUT_is_312.5MHz-156.25MHz
 - XO input = 48 MHz from SMA100B
 - Output = 312.5 MHz on OUT[7:0] and 156.25 MHz on OUT[15:8]
 - Data contains phase noise plots with and without 4 MHz high-pass filter (HPF) applied
 - LMK5B33216_ConfigAndData_REF_is_None_XO_is_48MHzSMA100B_OUT_is_312.5MHz-50MHz_A
 - XO input = 48 MHz from SMA100B
 - Output = 50 MHz on OUT[7:0] and 312.5 MHz on OUT[15:8]
 - Data contains phase noise plots with and without 4 MHz high-pass filter (HPF) applied
 - LMK5B33216_ConfigAndData_REF_is_None_XO_is_48MHzSMA100B_OUT_is_312.5MHz-50MHz_B
 - XO input = 48 MHz from SMA100B
 - Output = 50 MHz on OUT[1:0], OUT[13:8] and 312.5 MHz on OUT[7:2], OUT[15:14]
 - Data contains phase noise plots with and without 4 MHz high-pass filter (HPF) applied
 - LMK5C33414A
 - LMK5C33414A_Config_REF_is_1PPS_XO_is_48MHz_OUT0_is_1PPS
 - XO input = 48 MHz
 - IN0 input = 1PPS CMOS
 - Output = 1PPS CMOS on OUT[1:0]

5.2 Version 2025-01-23

- Added Configuration Files and Data
 - LMK5B33216
 - LMK5B33216_ConfigurationAndData_REF_is_None_XO_is_48MHzSMA100B_OUT_is_312.5MHzDPLL reference = 25 MHz from SML01
 - XO input = 48 MHz from SMA100B
 - Output = 312.5 MHz
 - Data contains phase noise plots with and without 4 MHz high-pass filter (HPF) applied

5.3 Version 2024-11-22

- Added Configuration Files and Data
 - LMK5B33216
 - LMK5B33216_ConfigurationAndData_REF_is_25MHzSML01_XO_is_48MHzLMK6C_OUT_is_625MHz
 - DPLL reference = 25 MHz from SML01
 - XO input = 48 MHz from SMB100A
 - Output = 625 MHz
 - Data contains phase noise plots with and without 4 MHz HPF applied
 - LMK5B33216_ConfigurationAndData_REF_is_25MHzSML01_XO_is_48MHzSMB100A_OUT_is_625MHz

- DPLL reference = 25 MHz from SML01
- XO input = 48 MHz from LMK6C oscillator
- Output = 625 MHz
- Data contains phase noise plots with and without 4 MHz HPF applied

5.4 Version 2024-11-19

- First release
- Added Configuration Files
 - LMK5B33216
 - LMK5B33216_Configuration_ROM0_to_ROM8
 - LMK5C33216A
 - LMK5C33216A_Configuration_ROM0_to_ROM8

6 Known Issues

None

7 Technical Support and Product Updates

Please post questions for support on to the TI E2E Community at <https://e2e.ti.com/support/clocks/>

8 Release History

Doc No.	Version	Description	Release Date
4	2025-01-30	Added LMK5B33216 configuration files and data Added LMK5C33414A configuration file	30 Jan 2025
3	2025-01-23	Added LMK5B33216 configuration files and data	23 Jan 2025
2	2024-11-22	Added LMK5B33216 configuration files and data	22 Nov 2024
1	2024-11-19	First Release Added LMK5B33216 configuration files	19 Nov 2024