MPEG2 Main Profile Decoder (v1.10.00) on DM6467

FEATURES

- eXpressDSP™ Digital Media (XDM 1.2 IVIDDEC2) complaint
- Validated on DM6467 EVM
- All I, P, and B frame decoding supported
- Both progressive and interlaced supported
- Outputs are available in YUV 420 interleaved formats (Y in one plane and U and V data interleaved to form the other plane)
- Frame based decoding with frame size being multiples of 16 supported
- Simple Profile MPEG2 decoding supported
- Main Profile MPEG2 decoding supported
- DMA based framework supported
- Use of C64x+ and ARM968 of HD-VICP0 and HDVICP1 supported
- Interrupt based communication between processors supported
- Bottom field optimization option added for B Frames
- Output frames are available in display and decode order
- DeBlocking and Deringing supported

DESCRIPTION

MPEG2 video standard specifies the decompression and coded representation for entertainment-quality digital video. It is validated on DM6467 EVM, with Code Composer Studio version 3.3.49, and code generation tools version 6.0.16.

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Performance Summary

This section describes the performance of the MPEG2 Decoder on DM6467 EVM.

Table 1. Configuration Table

CONFIGURATION	ID
Mpeg2 Main Profile at High Level (no De-blocking)	DM6467_MP_001
Mpeg2 Main Profile at High Level (with De-blocking + De-ringing)	DM6467_MP_002

Table 2. Cycles Information in MHz - Profiled on DM6467 EVM with Code Generation Tools Version 6.0.16

CONFIGURATION ID	TEST DESCRIPTION	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND)[1] [2]			
		DSP CYCLES AT 600 MHZ		HDVICP ARM 968 CYCLES AT 300 MHz	
		AVERAGE	PEAK[3]	AVERAGE	PEAK[3]
DM6467_MP_001	1080i25_shields_ter_1920x1080_420_bf.m2v	6.4	6.8	246	259
	1080i25_stockholm_ter_1920x1080_420_bf.m2v	6.4	6.8	240	253
	mobcal_ter_1920x1080_420_br_3_10.m2v (B-Frames in sequence)	6.3	6.7	263	314
DM6467_MP_002	1080i25_shields_ter_1920x1080_420_bf.m2v	6.7	7.0	273	280
	1080i25_stockholm_ter_1920x1080_420_bf.m2v	6.7	7.0	267	274
	mobcal_ter_1920x1080_420_br_3_10.m2v (B-Frames in sequence) DSP cycles at 600 MHz	6.6	7.0	292	336

(1) Measured with program memory, stack, and I/O buffers in external memory and with cache configuration 32 K bytes L2 cache, 32 K L1D cache and 32 K L1P cache.
(2) Average and peak MCPS measurements can vary by +/-5%.
(3) Peak values are calculated assuming that the most demanding frame is repeated 30 times in the sequence, rather than finding the most demanding 30 frames sequence in the bit-stream.

Table 3. Memory Statistics - Generated with Code Generation Tools Version 6.0.16

CONFIGURATION ID	MEMORY STATISTICS[1]				TOTAL
	PROGRAM MEMORY	DATA MEMORY			
		INTERNAL[2]	EXTERNAL[2]	STACK	
DM6467_MP_001 DM6467_MP_002	59.5	32	29.4	2	123.3

(1) All memory requirements are expressed in kilobytes (1K-byte = 1024 bytes).
(2) Internal memory is placed in L2 SRAM.

Table 4. Internal Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY - INTERNAL [1]		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
DM6467_MP_001 DM6467_MP_002	0	32	0

(1) All memory requirements are expressed in kilobytes

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Table 5. External Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY - EXTERNAL [1]		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
DM6467_MP_001 DM6467_MP_002	0.50	0	27.76

(1) All memory requirements are expressed in kilobytes.

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Notes

The performance values in tables 2, 3, and 4 is a result of the following configuration:

- HDVICP
  - The entire HDVICP is a video resource and uses 16K ITCM and 8K DTCM.
  - The decoder is configured to run on either HDVICP-0 or HDVICP-1
- Cache configuration

Table 6. Cache Configuration

	AVAILABLE	USED
L1 P (Program Memory)	32K	32K - cache
L1 D (Data Memory)	32K	32K - cache
L2	128K	32K - cache

- DMA configuration

Table 7. DMA Configuration

TC Q's	TC 0	TC 1	TC 2	TC 3	TOTAL
Usage	Writes to L2	Not used	Writes to HDVICP and DDR	Writes to HDVICP and DDR	
Priority	2 (default)	-	2 (default)	2 (default)	
EDMA Channels	1	-	7	9	17/64
QDMA Channels	0	-	0	0	0/8
Num PARAMs	-	-	-	-	168/512

- Code placement

  All the algorrithm code are placed in external memory. The performance values in table 2, 3, and 4 are sensitive to algorithm code placement. See the sample linker file provided in the test application setup for algorithm code placement.

References

- *MPEG2 Main Profile Decoder on DM6467 User's Guide* (literature number - SPRUFE1A)

Glossary

TERM	DESCRIPTION
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

ACRONYM	DESCRIPTION
CPB	Constrained Parameters Bit-streams
DMA	Direct Memory Access
DMAN3	DMA Manager
EVM	Evaluation Module
IDCT	Inverse Discrete Cosine Transform
MCPS	Mega Cycles Per Second
MPEG	Motion Picture Expert Group
QDMA	Quick Direct Memory Access
XDM	eXpressDSP Digital Media

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Revision History

This Data sheet revision history highlights the changes made to the SPRS481A codec specific Data sheet to make it SPRS481B.

Table 8. Revision History for MPEG2 Main Profile Decoder on DM6467

SECTION	CHANGES
Table 7	• Modified DMA Configuration values

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